Sigma Journal of Engineering and Natural Sciences
Web page info: https://sigma.yildiz.edu.tr
DOI: 10.14744/sigma.2026.2161

Research Article

Comparative analysis of multi-carrier pulse width modulation schemes on dynamic performance evaluation of cascaded H-bridge medium voltage STATCOM

Ahmet Mete VURAL[1,*]

[1]*Department of Electrical and Electronics Engineering, Gaziantep University, Gaziantep, 27310, Türkiye*

ARTICLE INFO

Article history
Received: 15 March 2025
Revised: 28 April 2025
Accepted: 10 July 2025

Keywords:
Capacitor Voltage Balancing;
Carrier-Based PWM Scheme;
Harmonic Evaluation;
Semiconductor Losses;
STATCOM

ABSTRACT

This paper presents a comprehensive comparative analysis of various multi-carrier pulse width modulation (PWM) techniques in the context of a medium-voltage cascaded H-bridge (CHB) static synchronous compensator (STATCOM). The study evaluates four commonly used carrier-based PWM methods with respect to key performance metrics, including semiconductor losses (conduction and switching), capacitor voltage balancing capability, current harmonic distortion, and the dynamic performance of the decoupled dq current controllers. These PWM methods are phase disposition (PD), phase opposition disposition (POD), alternative phase opposition disposition (APOD) as level-shifted PWM (LS-PWM), and phase-shifted PWM (PS-PWM). A detailed simulation model of a three-phase 11-level CHB-STATCOM operating at 11 kV and ±3.8 MVAR is developed to systematically assess each modulation scheme across different carrier frequencies. The results reveal that while LS-PWM techniques (PD, POD, APOD) offer lower semiconductor losses, they suffer from poor natural capacitor voltage balancing and inadequate harmonic performance at lower frequencies. In contrast, PS-PWM provides superior capacitor voltage balancing and harmonic reduction, even without auxiliary control mechanisms, albeit at the cost of increased switching losses. Quantitative analysis using two performance metrics confirms that higher carrier frequencies negatively impact the dynamic response of the current controllers. The findings suggest that PS-PWM with moderate switching frequency (0.5-1.0 kHz) is the most practical choice when considering all performance criteria holistically. This study contributes to establishing a systematic PWM selection framework for CHB-STATCOM applications in medium-voltage power systems.

Cite this article as: Vural AM. Comparative analysis of multi-carrier pulse width modulation schemes on dynamic performance evaluation of cascaded H-bridge medium voltage STATCOM. Sigma J Eng Nat Sci 2026;44(5):3338–3356.

***Corresponding author.**
*E-mail address: mvural@gantep.edu.tr

This paper was recommended for publication in revised form by Editor-in-Chief Ahmet Selim Dalkilic

Published by Yıldız Technical University Press, İstanbul, Turkey
© Author. This is an open access article under the CC BY-NC license (http://creativecommons.org/licenses/by-nc/4.0/).

INTRODUCTION

Static synchronous compensator (STATCOM) is a member of second-generation Flexible AC Transmission System (FACTS) family that is shunt-connected to the power system through a coupling transformer or a reactor [1], [2]. Its main applications include dynamic reactive power and voltage control, harmonic mitigation, and damping of power oscillations [3, 4]. STATCOM can be implemented using either a current-source converter (CSC) topology or a voltage-source converter (VSC) topology [5]. Studies show that VSC-based STATCOM has better harmonic performance, faster response time, and lower operating voltages when compared to CSC-based STATCOM [6]. The VSC converts DC voltage waveform into the three-phase AC voltage waveform at the fundamental frequency. This AC voltage can be controlled by adjusting amplitude and phase angle. This property allows STATCOM to generate or absorb controllable reactive power so that the voltages can be controlled and stabilized in power systems. Among VSC-based topologies, the cascaded H-bridge (CHB) topology has many advantages due to its multilevel voltage generation capability that can provide high-quality voltage output. Also, with reduced voltage stress on its semiconductors and modularity, this topology can be practically applied to STATCOM systems [7, 8]. On the other hand, carrier-based pulse width modulation (PWM) technique plays a critical role in power electronic systems. PWM technique can effectively control the output voltage, phase angle, as well as the fundamental frequency of VSCs [9]. Sinusoidal PWM is one of the types of PWM techniques which is characterized by its sinusoidal reference signal. It is widely used in the industry for its low harmonic distortion. The literature has some studies about the loss calculations for STATCOM and comparison among different PWM schemes. In [10], various degree bus clamping PWM techniques are compared with space vector (SV) PWM in terms of power conversion losses. The STATCOM power levels vary between 100 and 150 kVA. In [11], a simulation-based study is carried out which is about the evaluation and comparison of semiconductor losses in VSC and CSC-based STATCOM under voltage imbalance conditions. Results indicate that under full load conditions, VSC-STATCOM demonstrates lower efficiency compared to CSC topology. In [12], direct current controllers and PWM controllers in a grid-connected two-level converter are investigated and compared in terms of semiconductor losses under the same operating points and the same average switching frequency. The converter is examined when it injects both active and reactive power to the grid. Experimental results demonstrate that direct current controllers can reduce the converter's total losses. In [13], nearest level control is found to have lower semiconductor losses compared to phase shift (PS)-PWM method in modular multilevel converter (MMC) STATCOM. In [14], a loss analysis, conducted through simulations and experiments, is presented for a CSC-STATCOM using selective harmonic elimination method to decrease switching frequency. It is shown that the DC current level significantly impacts power losses. In [15], a novel carrier-based modulation technique for a three-level neutral point clamped STATCOM is proposed to achieve an even power loss redistribution. Additionally, the capacitor voltages are balanced via an active neutral point voltage balancing control. A simulation-based framework aimed at reducing losses and harmonics in a three-phase delta-connected 13-level CHB-STATCOM is presented in [16]. Square-wave control is employed for the power semiconductors to minimize both switching losses and DC voltage ripple. Optimal system parameters are theoretically derived and validated through simulations. While key performance aspects of the STATCOM are addressed, the study does not include a comparative analysis of common PWM methods. Additionally, only conduction losses are considered, with switching losses omitted from the evaluation. In [17], a hybrid structured CHB-STATCOM with reduced count of semiconductors is suggested with a hybrid modulation scheme to reduce the switching losses. The proposed topology with the hybrid modulation method is compared in terms of semiconductor losses and harmonic content as well as capacitor voltage balancing control with conventional approach. In [18], double-star half-bridge and single-delta full-bridge MVA scale MMC-STATCOM configurations are presented and compared in terms of cost as well as conduction and switching losses. However, harmonics and voltage balancing are not considered. As seen in the studies mentioned above, there is no existing work that compares common level and PS-PWM methods in terms of semiconductor losses, total harmonic distortion (THD), as well as capacitor voltage balancing, as intended in this study. On the other hand, effective capacitor voltage balancing remains a crucial challenge in STATCOM applications [19]. In [20], a voltage balancing control method employing modified zero-sequence voltage injection is utilized for a wye-connected CHB-STATCOM. To alleviate the computational burden, the zero-sequence voltage is expressed as a DC variable within the dq frame. Furthermore, the study in [13] compares nearest level control with the PS-PWM method concerning submodule capacitor voltage balancing in a 15 MVA MMC-STATCOM during both positive and negative sequence current injections. Nearest level control has demonstrated comparable performance to the PS-PWM scheme in balancing capacitor voltages. The study in [21] proposes an inter-cluster DC capacitor voltage balancing control scheme for MMC-STATCOMs under unbalanced grid conditions. This approach involves injecting both negative-sequence current and zero-sequence voltage into the phase limbs of the MMC. A topology based on diode clamping circuit for a STATCOM is suggested in [22] to equalize the voltages across all capacitors in each phase. Simulation and experimental case studies show that the proposed solution

improves the balancing speed and performance compared to software-based approaches. To cope with unbalance during grid fault conditions, a zero-sequence voltage control strategy is proposed in [23] for a star-connected CHB-STATCOM to balance the voltages of the DC link capacitors. A self-stabilizing algorithm is proposed in [24] to achieve voltage balancing control of a star-connected CHB-STATCOM by linearly adjusting the negative sequence modulation reference voltages in the dq reference frame. In [25], a carrier rotation scheme combined with the PS-PWM method is proposed to achieve dynamic active power balancing among the modules in a three-phase CHB-STATCOM. By this way, the capacitor voltages remain balanced without the need for individual voltage control or auxiliary circuits. In [26], the selective harmonic elimination (SHE) technique is applied to a three-phase, five-level CHB-STATCOM with unequal DC-link voltages across the H-bridge cells. Both simulation and experimental results confirm that the proposed SHE-based modulation successfully regulates the individual capacitor voltages to their respective reference values. A technique utilizing zero-sequence voltage and negative-sequence current is proposed for the CHB-STATCOM to enable operation under asymmetrical conditions caused by power system faults [27]. The results demonstrate that the capacitor voltages among phase clusters remain balanced under fault conditions. An individual voltage balancing strategy suitable for PWM techniques is presented in [28] for CHB-STATCOM applications. This strategy ensures that the delivered reactive power is evenly distributed among all H-bridge cells of the converter. A self-capacitor voltage balancing method for CHB-STATCOM, based on hybrid modulation that combines selective harmonic elimination (SHE) and carrier-based PWM along with redundant switching state swapping, is proposed in [29]. A unified approach for designing the control loops of a delta-connected 90 MVA CHB-STATCOM is proposed in [30], addressing capacitor voltage regulation, voltage balancing, circulating current suppression, and reactive power control at the point of common coupling (PCC). Previous publications present either an additional control algorithm, modification of switching method, or an additional circuit to cope with capacitor voltage balancing in STATCOM. However, they lack the investigation of natural voltage balancing abilities of various common PWM schemes. Moreover, no semiconductor loss and harmonic content analysis is addressed in these studies. In this respect, this study aims to investigate natural voltage balancing abilities of common PWM schemes and consolidates PWM selection criterion based on key performance metrics namely, semiconductor losses (conduction and switching), natural capacitor voltage balancing capability, and harmonic reduction at the output of a three-phase star-connected medium voltage CHB-STATCOM. The carrier-based PWM schemes considered in this work are phase displacement (PD)-PWM, phase opposition displacement (POD)-PWM, alternative phase opposition displacement (APOD)-PWM, and PS-PWM. Despite the importance of the aforementioned performance parameters, the literature reveals that their combined evaluation for choosing the carrier-based PWM scheme for CHB-STATCOM control has received limited attention. Furthermore, Table 1 summarizes how this work differs from similar studies in the literature in the context of PWM comparison for CHB based inverter and STATCOM applications. It is evident that there is no study that considers three-performance metrics together as done in this work [31-38].

With the support of the literature review presented above, the contributions of this work can be summarized as follows;

1. A comparative analysis of various carrier-based level and phase-shifted PWM methods based on semiconductor losses, THD, and natural voltage balancing capability has been carried out for medium voltage CHB-STATCOM.
2. The conduction losses and switching losses for IGBTs and diodes have been separately analyzed and compared when CHB-STATCOM is operated under different PWM schemes. The loss curves are fitted from the datasheet of the semiconductors.
3. Together with the above comparisons, the dynamic performances of decoupled current controllers of STATCOM have been quantitatively evaluated using two performance indices.

The paper is organized as follows: Section 2 introduces the system description, including the power circuit topology of the STATCOM and power stage system parameters. Section 3 provides an overview of the carrier-based PWM methods used in multilevel converter topologies. Section 4 explains how the semiconductor losses are calculated for IGBTs and diodes. Section 5 presents simulation results for comparisons, accompanied by relevant discussions. Finally, Section 6 summarizes the key findings of this study.

SYSTEM DESCRIPTION

The power circuit configuration of the three-phase CHB-STATCOM, connected to an 11 kV grid at PCC, is depicted in Figure 1. Each phase of the STATCOM comprises five cascaded H-bridges. Each H-bridge incorporates four IGBT switches and a DC link capacitor, C. The voltage across this capacitor is regulated to a reference value E_{ref} by the STATCOM control system. With each H-bridge capable of producing three voltage levels ($-E$, 0, $+E$), the cascaded structure in each phase generates an 11-level staircase voltage waveform at full modulation index. This significantly reduces the harmonic distortion of STATCOM current. An L-filter is used to couple the STATCOM output to the grid. Reactive power flow, Q_S, is governed by the interaction between the AC grid voltage and the STATCOM output voltage. When the STATCOM voltage, V_C, exceeds the grid voltage, V_g, the STATCOM acts as a capacitor, injecting

Table 1. PWM comparison studies in the literature for CHB based inverters and STATCOM

Investigated topology	STATCOM functionality	Compared modulation schemes	Switching frequency	Investigated performance metrics	Reference
3-phase 5-level	yes	PS-PWM PD-PWM 3rd harmonic injected PS-PWM SV-PS-PWM SV-PD-PWM	1.2 kHz	voltage balancing current THD **no loss comparison**	[31]
1-phase 5-level	no	PD-PWM POD-PWM APOD-PWM	0.5 – 4.0 kHz	voltage THD **no loss comparison**	[32]
5-level	no	PD-PWM POD-PWM APOD-PWM	2.0 kHz	voltage THD **no loss comparison**	[33]
3-phase 21-level	no	PD-PWM PS-PWM	8.0 kHz	voltage THD **no loss comparison**	[34]
3-phase 5-level	yes	PD-PWM POD-PWM APOD-PWM PS-PWM	5.0 kHz	no voltage balancing voltage, current THD **no loss comparison**	[35]
3-phase 5-level	yes	PS-PWM PS-PWM with 3rd harmonic injection	1.2 kHz	no voltage balancing current THD **no loss comparison**	[36]
3-phase 5-level	no	POD-PWM APOD-PWM PS-PWM with 3rd harmonic injection	Not specified	voltage THD **no loss comparison**	[37]
3-phase 9-level	no	PD-PWM POD-PWM APOD-PWM PS-PWM	Not specified	voltage THD **no loss comparison**	[38]
This study 3-phase 11-level	yes	PD-PWM POD-PWM APOD-PWM PS-PWM	0.5-5 kHz	voltage balancing current THD losses compared	

reactive power ($Q_S > 0$) into the grid. Conversely, if V_C is lower than V_g, the STATCOM operates as an inductor, absorbing reactive power ($Q_S < 0$) from the grid. The power stage parameters used in the simulation studies are detailed in Table 2. The control system of STATCOM is schematically illustrated in Figure 2. It consists of two main blocks: "reference current generation" and "reference voltage generation". The reference current generation block serves as the outer controller. Within this block, the three-phase PCC voltages $V_{PCC(ABC)}$ are first fed into the PLL, which generates a synchronization signal, angle θ, ensuring that the STATCOM's output voltage is synchronized in both phase

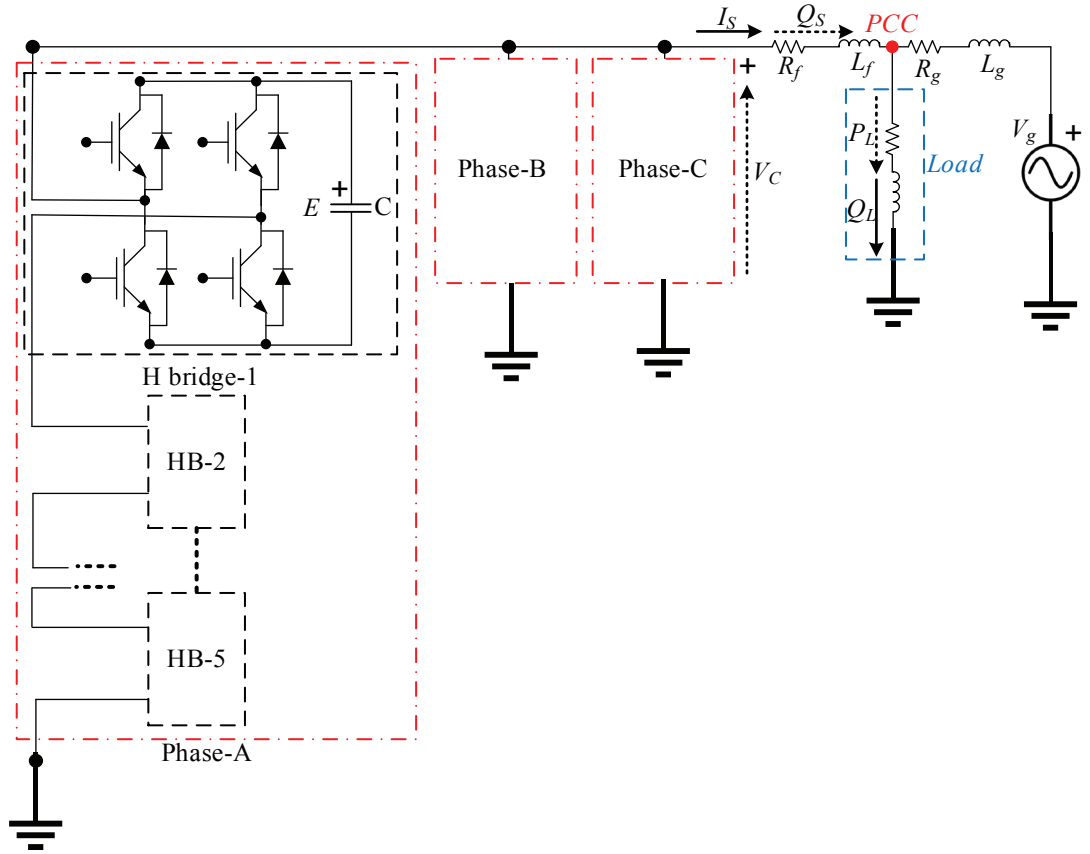


Figure 1. General circuit topology of a three-phase CHB-STATCOM connected to grid.

Table 2. The power stage parameters of the system

GRID parameter	Value	STATCOM parameter	Value
Voltage, V_g (LL)	11000 V	Rated reactive power, Q_S	±3.8 MVAR
Frequency, f	50 Hz	Rated voltage, V_C (ind. mode)	3565 V (LN)
Resistance, R_g	0.8929 Ω	Rated voltage, V_C (cap. mode)	7532 V (LN)
Inductance, L_g	0.01658 H	Rated current (inductive mode), I_S	280 A (rms)
Filter inductance, L_f	0.0121 H	Rated current (capacitive mode), I_S	188 A (rms)
Filter resistance, R_f	0.0764 Ω	DC link voltage, E	2245 V
Load real power, P_L	2.0MW	DC link capacitor, C	0.0015 F
Load reactive power, Q_L	1.5MVAR		

and frequency with the grid voltage. The system includes two coordinate transformation blocks (*abc*/*dq*) that convert three-phase quantities ($V_{PCC(ABC)}$, $I_{S(ABC)}$) into *dq* variables (I_d, I_q, V_d, V_q). The transformation matrix is expressed as follows [39]:

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (1)$$

where, θ represents the angle of the rotating reference frame, *a*, *b*, *c* are the three-phase quantities, and *d*, *q*, 0 are the constant quantities in the rotating reference frame.

The reference $I_{q\text{-}ref}$ is derived from the reference reactive power Q_{ref}. The reference $I_{d\text{-}ref}$ is determined by using a PI controller. This PI controller regulates the capacitor voltage E in each H-bridge by comparing the reference voltage E_{ref} with the average capacitor voltage E_{avg} of the STATCOM. The average value is calculated from individual measurements of capacitor voltages across each phase

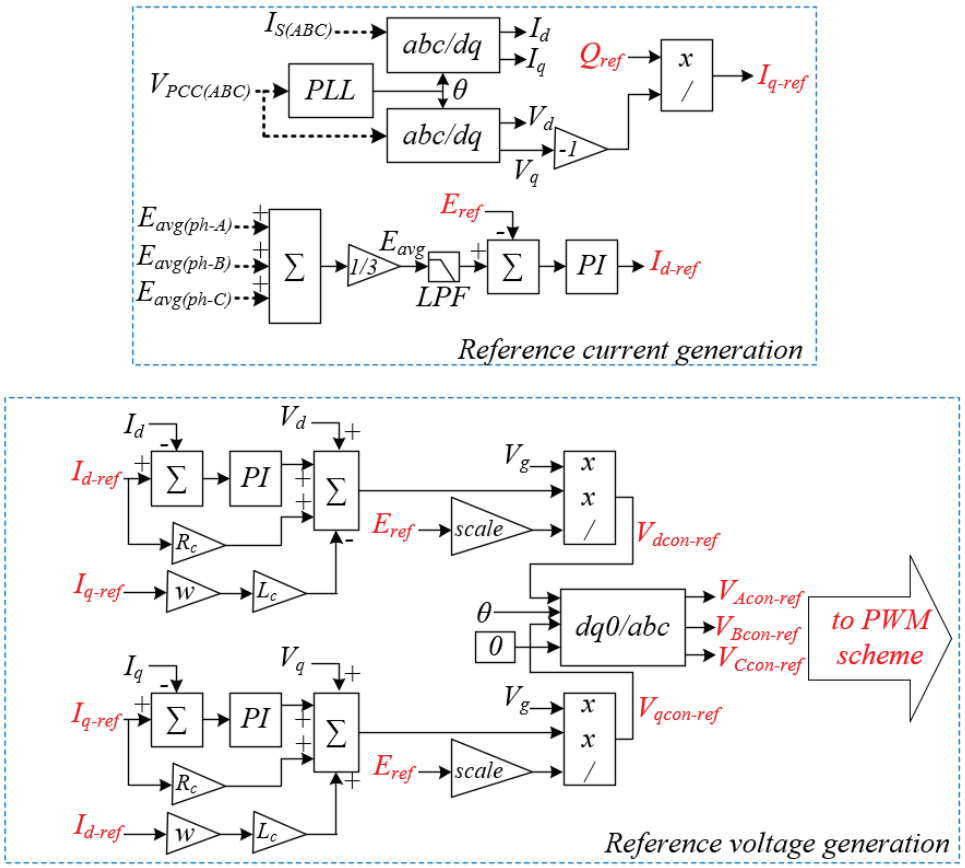


Figure 2. General control diagram of CHB-STATCOM. (a) Reference current generation blocks, (b) Reference voltage generation blocks.

of the STATCOM. The reference voltage generation block operates as the inner current controller. In the inner current controller scheme, the two PI controllers are used to track STATCOM's *dq* current components (I_d, I_q). The *d*-axis current controls the active power exchange between the STATCOM and the grid. The *q*-axis current controls the reactive power of the STATCOM that is injected or absorbed into the grid. The outputs of the controller are combined with various signals to achieve decoupled control. By this way, independent regulation of the STATCOM's real and reactive power is possible. Also, the dynamic response of the control system is improved. Finally, two voltage signals ($V_{dcon\text{-}ref}$, $V_{qcon\text{-}ref}$) are generated to produce three-phase reference voltage waveforms for PWM modulation. A block is used in order to perform the inverse coordinate transformation.

Modulation Techniques for Multilevel Converters

The modulation techniques for multilevel converter can be divided into four main groups. These are fundamental switching frequency, hybrid PWM, multicarrier PWM, and SV modulation techniques. The fundamental switching frequency technique can be divided into selective harmonic elimination (SHE) and nearest level control (NLC) types. On the other hand, the hybrid PWM group includes the nearest voltage control (NVC) method. Multicarrier PWM methods include both PS-PWM and level-shifted PWM (LS-PWM). LS-PWM is generally subdivided into three types. These are PD-PWM, POD-PWM, and APOD-PWM. Table 3 summarizes the common PWM techniques used in multilevel converters. Their description and advantages are also given in Table 3. High-frequency carrier-based switching schemes are popular due to their control advantages. In these methods, the carrier signals can be shifted either horizontally or vertically along the time axis. The carrier signal is then compared with a sinusoidal reference waveform. If the vertical adjustment is used, this technique is known as LS-PWM which includes PD-PWM, POD-PWM, and APOD-PWM types [40]. In PD-PWM, all the carriers are in phase. In POD-PWM, the carriers above and below the zero reference are 180° out of phase. In APOD-PWM, the adjacent carriers are 180° out of phase.

If the carriers are horizontally shifted, this technique is known as PS-PWM. Generally, the carrier-based switching methods require $n = 1$ carrier signals for an n-level converter. There are 11 voltage levels in each phase of the

Table 3. Summary of PWM techniques and theoretical benefits

PWM Technique	Description	Theoretical Benefits
Sinusoidal PWM (SPWM)	It modulates the pulse width according to a sinusoidal reference signal.	Simple implementation, low harmonic distortion at low modulation indices.
SVPWM	It utilizes SV theory to determine switching states in a 2D vector plane.	Higher DC bus utilization when compared to SPWM, lower THD.
Hysteresis PWM	It switches when the error between actual and reference current exceeds a hysteresis band.	Fast response, simple control, robust under dynamic conditions.
Delta PWM	It is a variant of hysteresis control which uses delta modulation to define the pulse width.	Simple control logic, good current tracking.
3rd harmonic injection PWM	It adds a 3rd harmonic to the reference signal to reduce harmonic content in the waveform.	High modulation index up to 1.15, better voltage utilization.
SHE-PWM	It calculates the switching angles to cancel specific harmonics.	It eliminates specific low-order harmonics, high-quality waveform.
Random PWM	It randomizes the switching instants to spread harmonics across the spectrum.	It reduces electromagnetic interference and audible noise by avoiding discrete harmonic peaks.
Double Edge PWM	It modifies both rising and falling edges of the switching pulses.	Lower switching losses, symmetric waveform.
PS-PWM	The phase is shifted to generate multiple PWM signals.	It reduces harmonics and losses especially in modular converters.
LS-PWM	It uses many carrier signals which are shifted in the voltage level.	It simplifies implementation for multilevel inverters, enhances voltage balancing; reduces THD in output voltage.
Hybrid PWM	It combines the benefits of different PWM techniques.	It offers the advantages of combining different PWM methods.

STATCOM configuration which is proposed in this study. So, 10 carrier signals should be used. The various carrier adjustments of the PWM schemes used in this study are shown in Figure 3.

Semiconductor Loss Calculation

The STATCOM system is capable of generating ±3.8 MVAR reactive power under rated conditions. The rated capacitor voltage for each H-bridge module is 2245V.

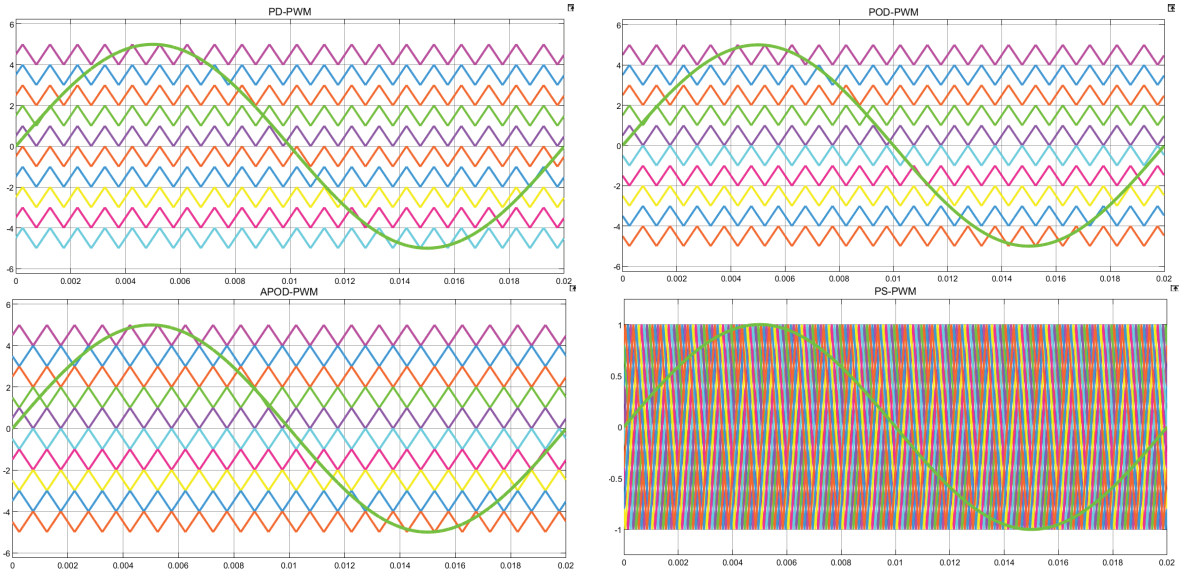


Figure 3. Reference waveform (green) and triangular carrier positions for various PWM schemes. (a) PD-PWM, (b) POD-PWM, (c) APOD-PWM, (d) PS-PWM.

The simulation studies show that the IGBTs in each H-bridge must withstand a repetitive current of 400A. The FD250R65KE3-K IGBT module from Infineon is selected to meet these requirements [41]. This IGBT module has a voltage rating of 6500V and a current rating of 250A. This IGBT is well-suited for medium-voltage converter applications which can offer a repetitive peak collector current of up to 500A and a collector-emitter voltage of up to 6500V. In this study, both the conduction and switching losses of this IGBT are analyzed and compared under various PWM schemes. The virtual junction temperature is assumed as 125 °C. The switching losses are generally divided into two categories. These are turn-on and turn-off losses. In this analysis, also the conduction and recovery losses of the reverse-parallel diode are taken into account. The other losses, such as gate driver losses and resistive losses outside of the semiconductors are neglected. To accurately compute switching losses in simulation studies, it is crucial to determine the exact turn-on and turn-off instants of each IGBT. This is achieved using rising and falling edge detectors, which identify these instants. The rising edge detector generates a pulse of magnitude 1 ($[RD] = 1$) when a logic signal of 1 turns the IGBT on. Conversely, $[RD]=0$ is produced when a logic signal of 0 turns the IGBT off. Accordingly, the power lost during the turn-on instant m of the IGBT is expressed as:

$$P_{ON[m]} = [RD] \times f_{onIGBT} \times V_{IGBT} \times {T_{sim}}^{-1} \quad (2)$$

where, V_{IGBT} is the IGBT voltage just before turning on, T_{sim} is the total simulation time, and f_{onIGBT} is a polynomial function which is fitted from the IGBT loss curve supplied by the manufacturer. This function is given as,

$$f_{onIGBT} = \left(\frac{1}{3600}\right) \times 0.01246 \times {I_C}^2 + 4.442 \times I_C + 297.7 \quad (3)$$

where, I_C is the IGBT collector current. The lost power at the turning off instant n of the IGBT is calculated as,

$$P_{OFF[n]} = [FD] \times f_{offIGBT} \times V_{IGBT} \times {T_{sim}}^{-1} \quad (4)$$

where, $[FD]$ takes a value of 1 if falling edge detector detects a turn off for IGBT, otherwise it remains 0. The polynomial function $f_{offIGBT}$ is obtained from the IGBT loss curve supplied by the manufacturer. This function is given as,

$$f_{offIGBT} = \left(\frac{1}{3600}\right) \times 5.605 \times I_C + 27.33 \quad (5)$$

Similarly, the recovery energy loss of the diode can be approximated using the following polynomial function, where I_F is the diode forward current and k is the turning off instant of the diode.

$$P_{REC[k]} = -\left(\frac{1}{3600}\right) \times 4.966 \times 10^{-7} \times {I_F}^3 - 0.003193 \times {I_F}^2 + 3.983 \times I_F + 218.6 \quad (6)$$

In order to calculate the conduction loss of the IGBT, the on-state resistance and forward voltage drop of this component should be determined from linearized current-voltage characteristics as given below,

$$I_C = 161.5 V_{CE} - 348.4 \quad (7)$$

where V_{CE} is the collector-emitter voltage of the IGBT. The reciprocal of the tangent of this line gives on-state resistance of the IGBT, R_{ON} = 0.00619195 Ω. The forward voltage drop of the IGBT can be calculated when I_C = 0, i.e., $V_{CE\,0}$= 2.15727554 volts. Similarly, the current-voltage characteristics of the diode taken from the datasheet can be linearized as shown below,

$$I_F = 219.9 V_F - 412.3 \quad (8)$$

where V_F is the forward voltage of the diode. The reciprocal of the tangent of this line gives on-state resistance of the diode, R_{ONd} = 0.00454752 Ω. On the other hand, the forward voltage drop of the diode can be computed by finding diode voltage when I_F = 0, i.e., $V_{F0} = 1.874943 V$. These two parameters are used to determine the conduction loss of the reverse-parallel diode during STATCOM operation. Finally, the conduction loss of each IGBT and diode are computed as follows,

$$P_{IGBT_C} = \frac{1}{T_{sim}} \sum_{i=1}^{n} \left[V_{CE0} I_{C+} R_{ON} {I_C}^2 \right] T_s \quad (9)$$

$$P_{diode_C} = \frac{1}{T_{sim}} \sum_{i=1}^{n} \left[V_{F0} I_{F+} R_{ONd} {I_F}^2 \right] T_s \quad (10)$$

Since the conduction losses are calculated using integration, (9) and (10) are actually performing numerical integration with a sample time of T_s = 1 μs. Finally, the total switching losses of the 60 IGBTs and 60 diodes in STATCOM (4 IGBTs/diodes in each H-bridge, 5 H-bridges in each phase, total 3-phases) are computed as follows,

$$P_{SW} = \sum_{i=1}^{60} \left(\sum_{i=1}^{M} P_{ON[i]} + \sum_{i=1}^{N} P_{OFF[i]} + \sum_{i=1}^{K} P_{REC[i]} \right) \quad (11)$$

where M, N, and K define the total turn-on or turn-off count of each semiconductor device. Similarly, the total conduction losses of the 60 IGBTs and 60 diodes are computed as follows,

$$P_{CON} = \sum_{i=1}^{60} \left(P_{IGBT_C(i)} + P_{diode_C(i)} \right) \quad (12)$$

Finally, all semiconductor losses are computed as follows,

$$P_{LOSSES} = P_{SW} + P_{CON} \quad (13)$$

Table 4 lists the semiconductor parameters used for calculating the switching and conduction losses in simulation studies.

Table 4. Semiconductor parameters

IGBT parameters @ T_j = 125 °C	Value	Diode parameters @ T_j = 125 °C	Value
V_f	2.15727554 V	V_f	1.874943 V
R_{on}	0.00619195 Ω	R_{on}	0.00454752 Ω
L_{on}	25 × 10^{-9} H	L_{on}	0 H
$R_{snubber}$	1 × 10^{6} Ω	v	500 Ω
$C_{snubber}$	250 × 10^{-9} F	v	250 × 10^{-9} F

Comparison Studies with Numerical Simulations

Before conducting comparison case studies, the STATCOM is simulated in both inductive and capacitive modes as the base case. The parameters listed in Table 2 and Table 4 are applied to all simulation studies. The simulation time step is set to 1 μs. The controller and filter parameters used in simulations are provided in Table 5. In this base case, the current controllers, as well as the DC voltage controller, are verified. It is also confirmed that the desired inductive (-) or capacitive (+) reactive power is injected into the grid. The PS-PWM switching scheme, with a carrier frequency of 1 kHz, is employed for the base case. Figure 4 illustrates the dynamic performance of the STATCOM controllers when the reactive power reference is changed at t = 0.5 s, transitioning from fully inductive (Q_{ref}= -3.8 $MVAR$) to fully capacitive mode (Q_{ref}= +3.8 $MVAR$). As depicted, between 0 and 0.5 s, the STATCOM's reactive power reference is negative, indicating that the STATCOM absorbs reactive power from the grid. After t = 0.5 s, the reactive power reference becomes positive, causing the STATCOM to inject reactive power into the grid. The dynamic responses of the i_q and i_d current controllers are presented in Figure 4 (a) and Figure 4 (b), respectively. Following an initial transient period of approximately 0.1 s, both currents closely track their reference values. Figure 4 (c) demonstrates that the average capacitor voltage (calculated from 5×3=15 capacitors, corresponding to 5 H-bridges in

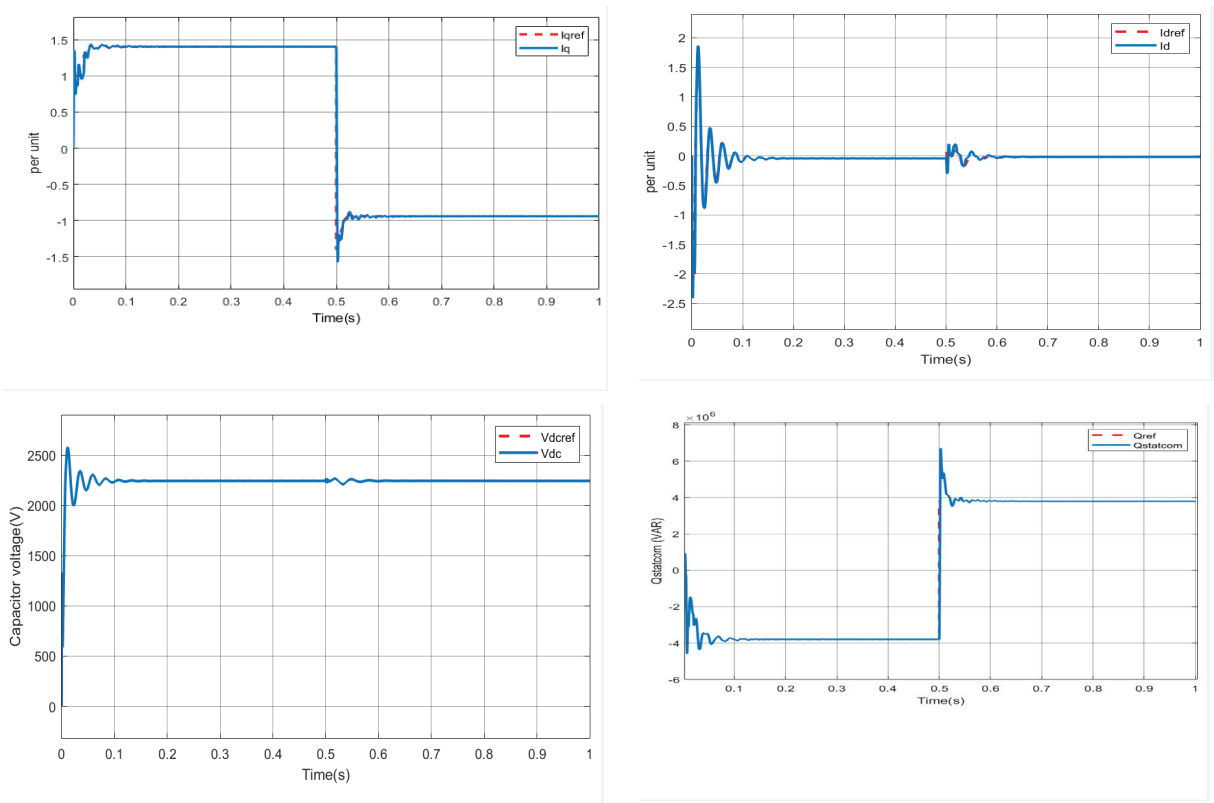


Figure 4. The transition from inductive to capacitive mode with a step change applied to reactive power reference at t=0.5s. (a) Dynamic response of Iq current controller, (b) Dynamic response of Id current controller, (c) Dynamic response of DC voltage controller, (d) Dynamic change of STATCOM reactive power.

Table 5. The controller and filter parameters for running STATCOM model

I_d and I_q current controller		DC voltage controller	
Parameter	**Value**	**Parameter**	**Value**
Proportional gain	0.8	Proportional gain	10
Integrator gain	8	Integrator gain	800
Low pass filter (for DC voltage measurement and dq transformation)			
Natural frequency		1.0 kHz	
Damping ratio		1.0	

each phase) smoothly follows its reference. These base case simulation results validate the effectiveness of the decoupled control strategy in independently regulating active and reactive powers. The STATCOM effectively responds to changes in reference currents while maintaining the average capacitor voltage stable at its reference value.

Semiconductor Loss Comparison

Since the STATCOM current is higher in inductive mode (due to the lower modulation index), the STATCOM is operated exclusively in inductive mode under rated conditions in this section, drawing 3800 kVAR of reactive power from the grid. Under these conditions, the IGBT current peaks at approximately 400A, and the continuous DC current per IGBT is measured at around 63A. Simulations indicate a startup transient lasting approximately 0.1 s when a unit-step reactive power reference is applied. Therefore, loss measurements are taken after this transient period. To ensure a fair comparison of PWM methods, no voltage balancing techniques such as closed-loop voltage control or switch swapping are employed. Figure 5 presents the total semiconductor

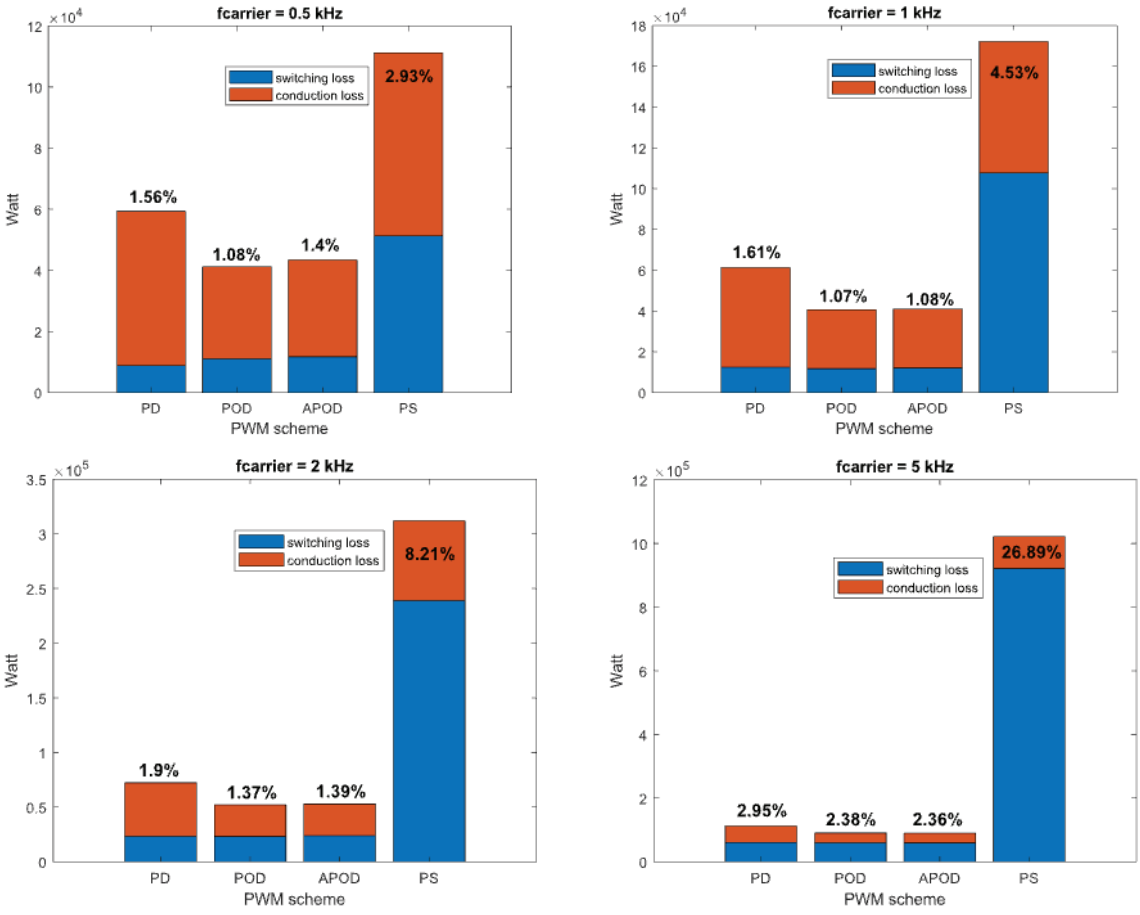
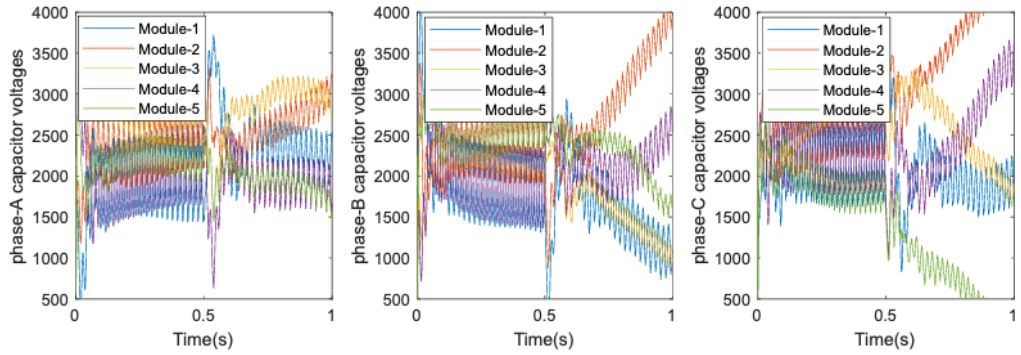


Figure 5. STATCOM semiconductor losses under various PWM schemes and carrier frequencies. (a) Carrier frequency is 0.5 kHz, (b) Carrier frequency is 1.0 kHz, (c) Carrier frequency is 2.0 kHz, (d) Carrier frequency is 5.0 kHz.

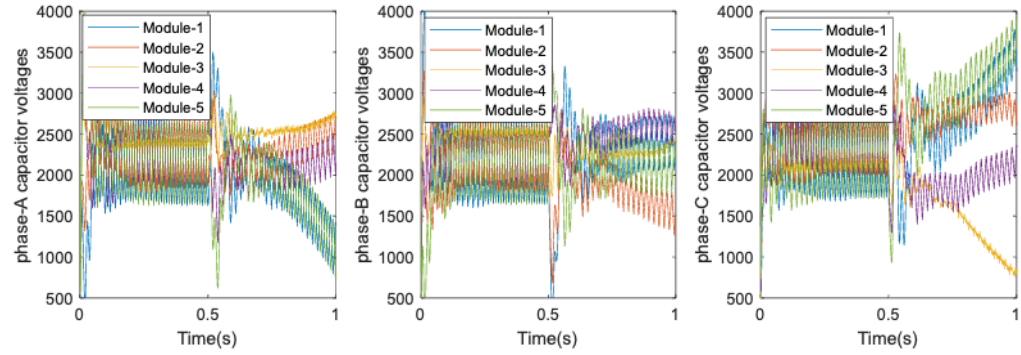
(IGBT and diode) losses of the three-phase STATCOM under various PWM schemes and carrier frequencies. Conduction and switching losses are shown separately, along with the percentage loss associated with each PWM scheme, relative to the STATCOM's rated reactive power. According to numerical simulations, the average semiconductor loss for LS-PWM schemes is approximately 1.68%. However, the PS-PWM scheme produces roughly 6.3 times more loss than LS-PWM, making its practical implementation challenging at high carrier frequencies. Nevertheless, PS-PWM has the advantage of evenly distributing power across the IGBTs, which supports natural capacitor voltage balancing. This aspect is analyzed in the next section. While LS-PWM schemes exhibit nearly identical switching losses, it is noteworthy that PD-PWM generates significantly higher conduction losses compared to other LS-PWM methods. In terms of total semiconductor losses, POD and APOD-PWM consistently achieve lower losses compared to PD-PWM. Based solely on efficiency criterion, POD or APOD-PWM may be preferred among all PWM switching schemes.

Comparison of Capacitor Voltage Balancing

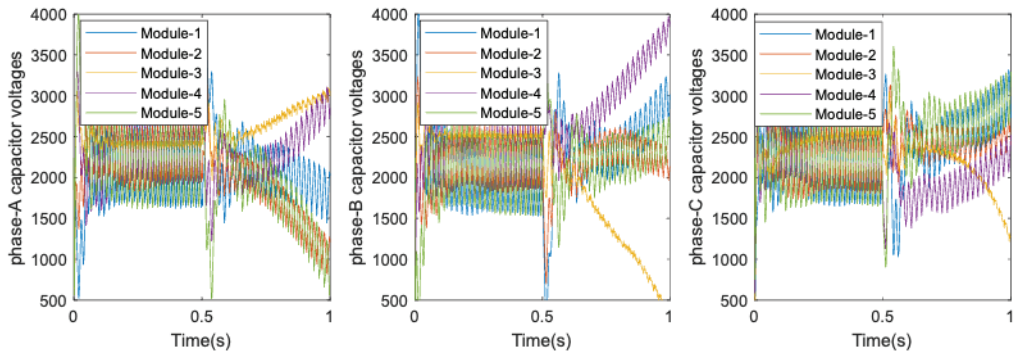
The designed STATCOM system consists of 5 H-bridges per phase. A total of 15 H-bridges is utilized. Consequently, 15 capacitor voltages must be controlled at the reference value of E_{ref} = 2245 V in inductive and capacitive modes of operation. In this section, the capacitor voltage balancing



(a) PD-PWM



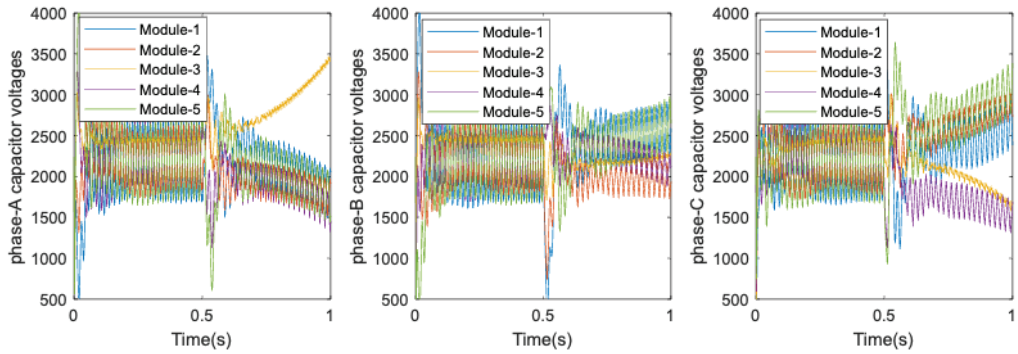
(b) POD-PWM



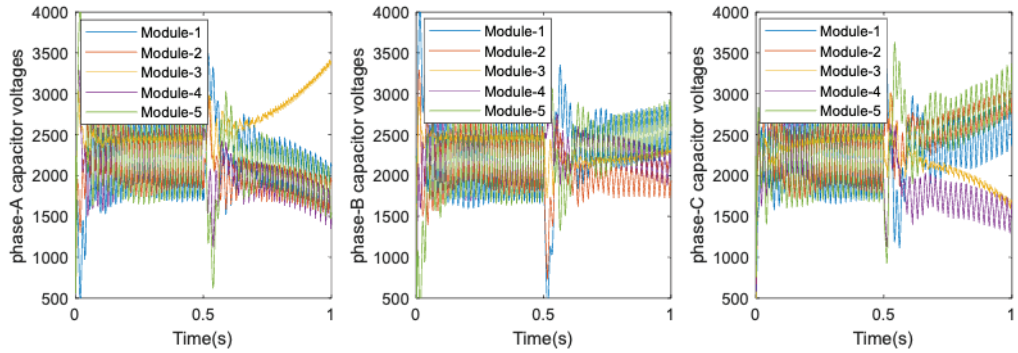
(c) APOD-PWM

Figure 6. Capacitor voltages of STATCOM in LS-PWM schemes at f_{car}= 1.0 *kHz*.

capabilities of various PWM techniques are analyzed at different carrier frequencies of f_{car} in both operating modes. For this analysis, the previously mentioned DC voltage controller is employed. This controller regulates the DC power input to the STATCOM by using a PI controller. This PI controller generates an error signal based on the average measurement of the 15 capacitor voltages. Here, the aim is to maintain all the capacitor voltages at their reference values as close as possible. Since no auxiliary voltage regulator or balancing algorithm is implemented, the voltage balancing performance of each PWM technique is compared individually. The transition is also studied to assess whether the DC controller, along with the respective PWM technique, is sufficient to maintain voltage balancing. To check the dynamic performance of the DC voltage controller in different PWM techniques, a transition from inductive to capacitive mode at $t = 0.5$s is generated. By this way, it would also be possible to assess the capability of the DC voltage controlle under different PWM schemes. Initially, the LS-PWM techniques are evaluated and compared at f_{car}= 1.0 *kHz*. The results are shown in Figure 6. The simulations at this carrier frequency reveal that none of the LS-PWM techniques (PD-PWM, POD-PWM, and APOD-PWM) achieved effective voltage balancing. In inductive mode, all the techniques exhibit unacceptable voltage ripples exceeding 20%. In capacitive mode, none of the techniques successfully maintains the capacitor voltages. The balancing could not be made. Such a response leads to the instability of the DC voltage controller. On the other hand, POD-PWM performs slightly better than PD-PWM in both inductive and capacitive modes. APOD-PWM shows similar results when compared to POD-PWM in inductive mode. But it fails to maintain the capacitor voltages in balance in capacitive mode. The findings from the simulations show that LS-PWM techniques are inadequate for DC capacitor voltage control and they are impractical for direct implementation. To investigate the impact of the carrier frequency, an additional case study is carried out by increasing the carrier frequency five times. The results are presented in Figure 7. When the carrier frequency is increased to 5.0 kHz, POD-PWM exhibits similar capacitor voltage fluctuations in inductive mode as observed at f_{car}= 1.0 *kHz*. In capacitive mode, the voltage deviations slightly decrease at f_{car}= 1.0 *kHz*. It is observed that increasing the carrier frequency from 1.0 to 5.0 kHz does not practically improve the capacitor voltage balancing for POD-PWM technique. Similarly, for APOD-PWM, increasing the carrier frequency to 5.0 kHz also generates a noticeable improvement over the results for previous carrier frequency. The key conclusions drawn from these simulation studies are that LS-PWM techniques are unsuitable for CHB-STATCOM applications due to their inability to stabilize the STATCOM controllers. Their dynamic



(a) POD-PWM

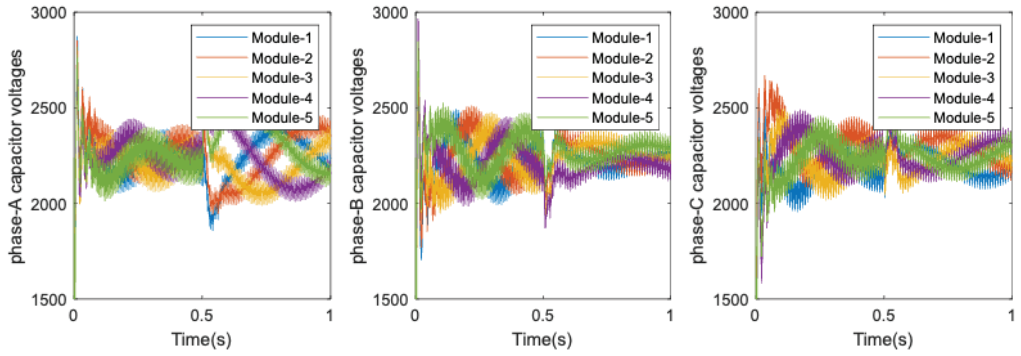


(b) APOD-PWM

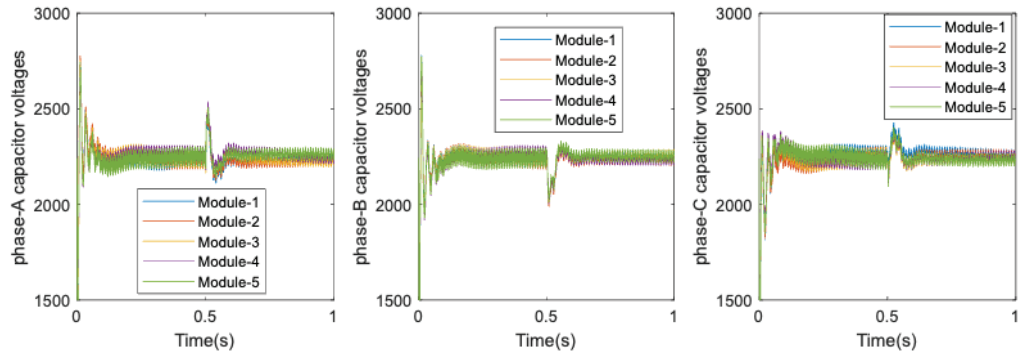
Figure 7. Capacitor voltages of STATCOM in two LS-PWM schemes at f_{car}= 0.5 *kHz*.

performance can be theoretically improved with additional controller or voltage balancing mechanisms. Another observation is that using a high carrier frequency does not provide substantial benefits when LS-PWM techniques are utilized.

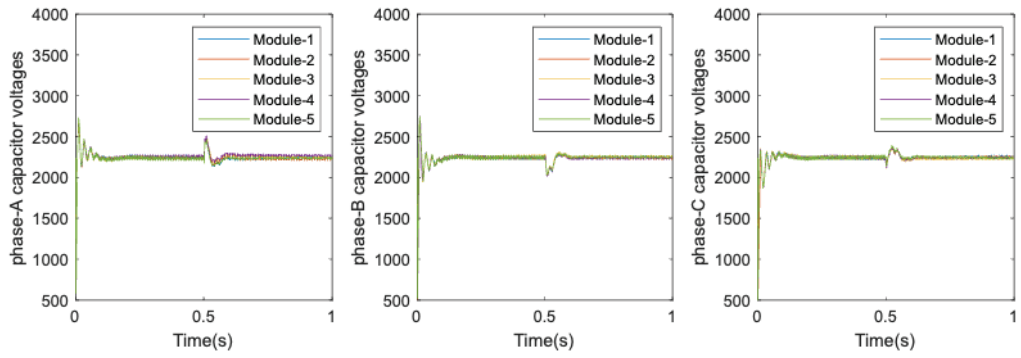
Given these observations, the performance of the PS-PWM technique in capacitor voltage balancing is investigated in this case study. Specifically, the dynamic voltage balancing performance of the PS-PWM technique is evaluated for three different carrier frequencies. The results, shown in Figure 8, indicate that PS-PWM method exhibits significantly better dynamic performance compared to LS-PWM techniques, effectively maintaining all capacitor voltages within a controlled ripple range in both inductive and capacitive modes. When comparing the two modes, PS-PWM method produces ripple voltages of approximately 20% in inductive mode and 4.45% on average in capacitive mode. Simulation results further reveal that even with a relatively low carrier frequency (f_{car}= 0.5 *kHz*), the STATCOM controllers operate with stable and satisfactory performance, despite the higher ripple voltages. To assess the impact of carrier frequency on dynamic voltage balancing, the carrier frequency f_{car} was increased to 2.0 kHz. In this scenario, the average ripple voltage decreased to approximately 2.25% compared to the previous case. Moreover, the study confirmed that further increasing the



(a) f_{car}= 0.5 *kHz*



(b) f_{car}= 1.0 *kHz*



(c) f_{car}= 2.0 *kHz*

Figure 8. Capacitor voltages of STATCOM during transition from inductive to capacitive mode in PS-PWM scheme.

carrier frequency to 5.0 kHz or higher would lead to additional reductions in ripple voltage. However, simulations at these higher frequencies were not pursued due to the excessive semiconductor losses associated with the PS-PWM technique at such operating conditions. Based on these results, it is demonstrated that PS-PWM method can be effectively applied in STATCOM systems without the need for additional voltage balancing controllers or algorithms, provided that an appropriate carrier frequency is selected with due consideration for the associated power losses. Additionally, it is shown that capacitor voltage ripples can be consistently maintained below 5% across all operating modes when PS-PWM method is employed.

Harmonic Reduction Comparison

In this section, the harmonic content of the STATCOM current is analyzed, and the PWM schemes are compared based on this criterion. According to IEEE Std 519 standards, the maximum allowable current THD in systems rated between 120 V and 69 kV is 5%, provided that the ratio I_{SC}/I_L <20 is satisfied. The grid has a short-circuit current of 2081.5A. The I_{SC}/I_L ratio is then calculated as 7.43 in inductive mode and 11.07 in capacitive mode, respectively. Since, these values are both less than 20, the standard requirement is met. In inductive mode, LS-PWM methods enable stable system operation despite high capacitor voltage ripple. However, in capacitive mode, the system becomes unstable when LS-PWM is used. This situation prevents reliable THD measurements. As a result, the THD evaluation for LS-PWM schemes is performed only in inductive mode of STATCOM. It can be concluded that the high ripple voltages observed in this mode cause increased THD. Although the system stability is maintained, the resulting THD values are still relatively high. As shown in Figure 9, only the PS-PWM method is able to maintain the STATCOM current THD below the 5% threshold under nominal loading conditions

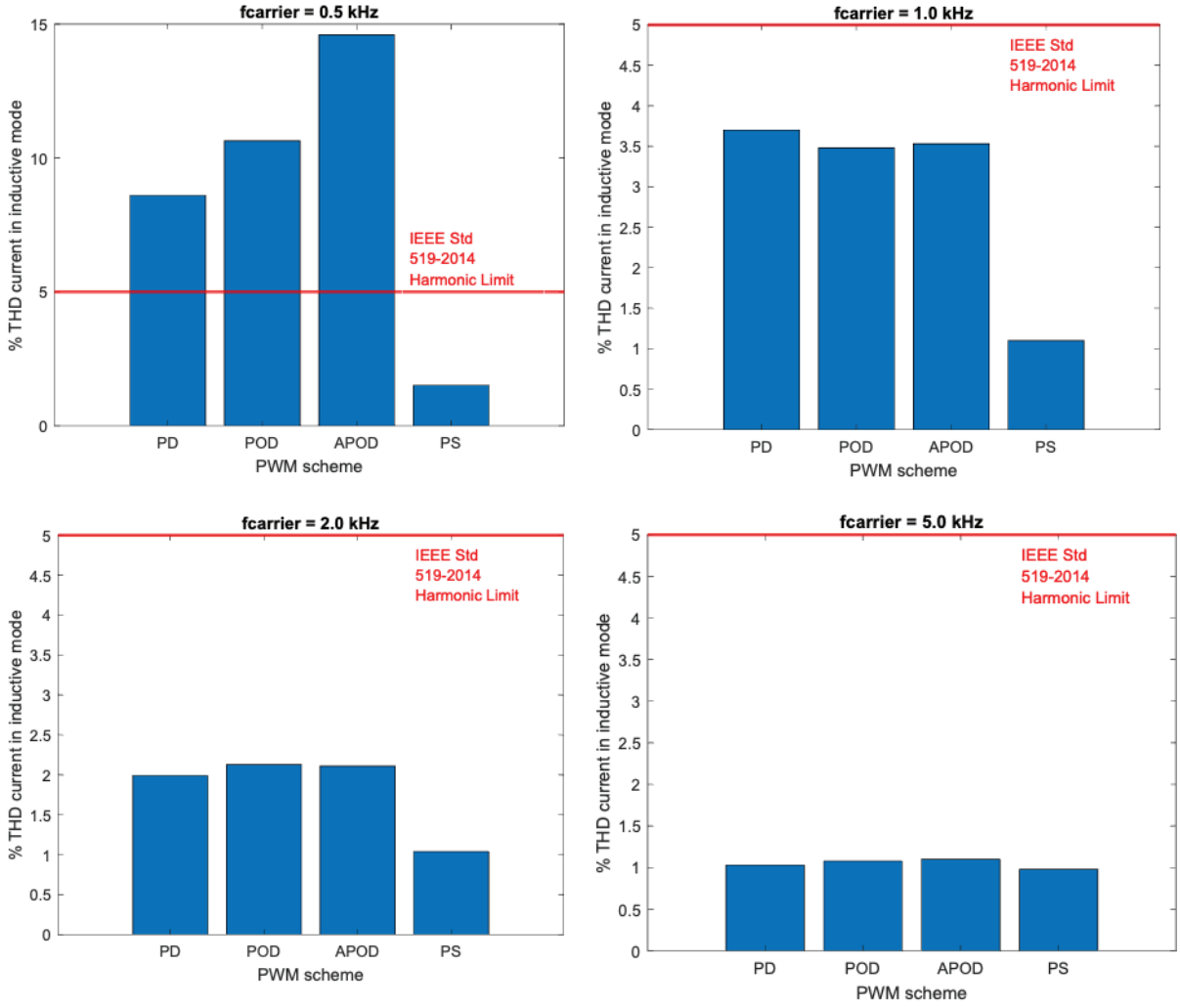


Figure 9. Percentage current THDs under various PWM schemes and carrier frequencies. (a) Carrier frequency is 0.5 kHz, (b) Carrier frequency is 1.0 kHz, (c) Carrier frequency is 2.0 kHz, (d) Carrier frequency is 5.0 kHz.

with I = 280 A. In this case, the STATCOM operates in the inductive mode at a carrier frequency of f_{car}= 0.5 kHz. In contrast, the LS-PWM methods fail to achieve acceptable THD performance at this frequency. It can be concluded that the placement of the carrier signals can significantly influence the harmonic content at the output. At the carrier frequency of f_{car}= 0.5 kHz, APOD-PWM method produces the highest current harmonics which reaches approximately to 15%. The POD-PWM and PD-PWM techniques come behind this value. At the carrier frequency of f_{car}= 1.0 kHz and above, all the PWM methods successfully maintain the current THD below 5% in inductive mode. Across all carrier frequencies except at f_{car}= 0.5 kHz, PS-PWM always demonstrates better performance compared to other methods. The PS-PWM always generates low current harmonics which comply with the IEEE standards. However, at f_{car}= 0.5 kHz, the performance gap narrows, and all methods produce comparable levels of current harmonics in practical terms. In conclusion, PS-PWM continuously delivers the lowest current harmonics in inductive mode, regardless of the carrier frequency. Also, it can be said that the PS-PWM method complies with the IEEE THD limits at the lowest carrier frequency.

Considering semiconductor losses, a lower carrier frequency is generally preferable. Since all PWM methods demonstrated comparable harmonic performance at higher carrier frequencies, any PWM method can be chosen when operating at that range. For capacitive mode of operation under nominal conditions (I = 188 A), only the harmonic performance of the PS-PWM method is analyzed, as none of the LS-PWM methods achieved adequate control performance in this mode. In case of the LS-PWM methods, the capacitor voltages could not be maintained at their reference values, as demonstrated in previous case studies, and the controllers failed to ensure stable operation. As shown in Figure 10, all carrier frequencies complied with IEEE standards, with only a minor exceedance of approximately 0.1% at f_{car}= 0.5 kHz. Since all carrier frequencies yielded similar current harmonics profiles, a relatively low carrier frequency would be preferable for the PS-PWM method when considering losses. However, if maintaining capacitor voltage balance is prioritized, a medium carrier frequency appears to offer the most appropriate compromise.

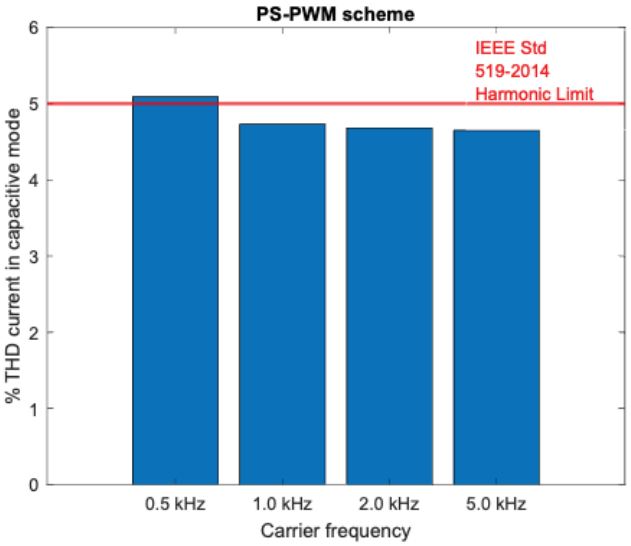


Figure 10. Percentage current THDs under various carrier frequencies with PS-PWM in capacitive mode.

EFfect of Carrier Frequency on Dynamic Performances of Current Controllers

In this section, the impact of carrier frequency on the dynamic performances of the dq current controllers of the STATCOM is investigated, specifically when the PS-PWM method is employed. To ensure consistency with previous case studies, the carrier frequency was varied from 0.5 kHz to 5 kHz. Only the PS-PWM method is considered in this analysis, as all LS-PWM methods were unable to maintain capacitor voltage balance in the STATCOM, as demonstrated in Section 5.2. A step change in the reactive power reference was applied at t=0.5, shifting the system from fully inductive operation (Q_{ref}= -3.8 $MVAR$) to fully capacitive operation (Q_{ref}= +3.8 $MVAR$). Meanwhile, the capacitor voltage reference of each H-bridge was maintained at E_{ref} = 2245 V. Under these conditions, it is observed that the dynamic responses of the current controllers remain qualitatively similar at different carrier frequencies. These responses resemble the behaviour depicted in Figure 4 (a) and (b). To perform a more detailed comparison, the dynamic tracking performance of the dq current controllers is quantitatively assessed. The results of this evaluation are presented in Figure 11. The performance is measured using the Integral of Squared Error (ISE) and the Integral of Time-weighted Squared Error (ITSE). These metrics are defined by the following equations,

$$ISE = \int_0^{T_{sim}} \left(I_{d(q)-ref} - I_{d(q)}\right)^2 dt \quad (14)$$

$$ITSE = \int_0^{T_{sim}} t\left(I_{d(q)-ref} - I_{d(q)}\right)^2 dt \quad (15)$$

These metrics are computed within the simulation environment over a total simulation time of T_{sim} = 1.0 s. To ensure a fair comparison, the PI controller parameters remained constant for all cases for all applied carrier frequencies. The ISE metric is generally used to evaluate the controllers' dynamic performance in tracking their reference values during startup. Also, ISE is used to evaluate the controllers' dynamic performance when the step change to the $Q_{ref}$is applied at t = 0.5 s. On the other hand, ITSE metric can measure the steady-state performance of the controllers by calculating greater errors over time. This makes ITSE especially useful for evaluating the long-term stability of the current controllers under different switching frequencies. The simulation results show that while both ISE and

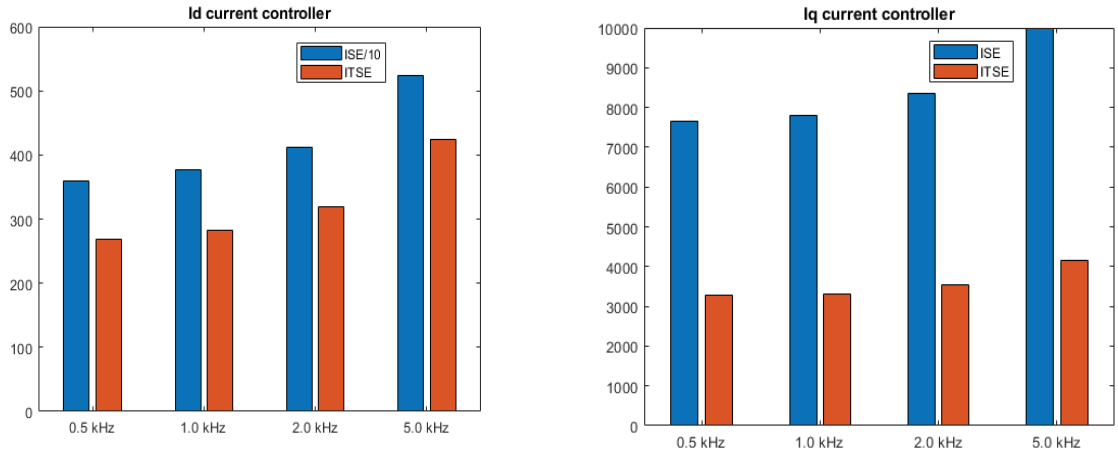


Figure 11. Quantitative evaluation of effect of carrier frequencies on dynamic performances of STATCOM current controllers. (a) Id current controller (b) Iq current controller.

ITSE values vary with the carrier frequency, there is a trade-off between the dynamic response and the steady-state performance. So, it can be concluded that when selecting an optimal carrier frequency, both rapid transient response and minimum steady-state error should be considered.

Based on the obtained numerical results, it can be concluded that the dq current responses are visually similar to each other at different carrier frequencies when the PS-PWM method is used. Both ISE and ITSE values increase with the higher carrier frequencies. This observation can indicate that an increase in the carrier frequency negatively impacts the dynamic performance of the controllers even they operate stable under steady-state conditions. The lowest ISE and ITSE values for both controllers are obtained at a carrier frequency of f_{car}= 0.5 *kHz*. It can be concluded that this frequency is the most favorable one that gives satisfactory dynamic and steady-state performance. The analysis also reveals that the Id current controller is relatively less sensitive to variations in the carrier frequency compared to the Iq current controller. This result can be explained such that the Iq control loop is more adversely affected by the higher switching frequencies. This is due to its more direct involvement in the reactive power regulation and its interaction with the STATCOM's capacitor voltage dynamics. The overall measurements show that when the PS-PWM is selected, the carrier frequency should be carefully adjusted. Because, the dynamic response and steady-state accuracy of the dq current controllers can be highly affected from the carrier frequency.

DISCUSSION ON COMPARATIVE STUDIES

This section gives a discussion on the overall simulation results when different PWM methods are used in STATCOM. The semiconductor switching losses, capacitor voltage balancing capability, current THD, and the dynamic performance of the dq current controllers are all considered.

1. When only the losses are considered, the LS-PWM methods can be preferred due to their lower switching characteristics. Among LS-PWM methods, the POD and APOD-PWM techniques produce lower semiconductor losses when compared to the PD-PWM method.
2. When the capacitor voltage balancing is considered, all LS-PWM methods have significant limitations. More specifically, the PD-PWM shows a weaker dynamic performance compared to POD and APOD-PWM. As demonstrated in the previous sections, these methods fail to regulate the capacitor voltages effectively under capacitive loading conditions. This condition is a major constraint for reliable STATCOM operation. Since, precise voltage control is very important for system stability and power quality.
3. The PS-PWM method can be recommended with a carrier frequency of either f_{car}= 0.5 *kHz* or 1.0 *kHz*. Without any supplementary controller or auxiliary circuit, the PWM method can meet the natural voltage balancing requirements. The carrier frequency of 1.0 kHz offers small ripple voltages. The higher carrier frequencies can achieve even lower ripple voltages.
4. When the STATCOM operates in inductive mode, it draws reactive power from the grid. In this operation mode, any PWM method can be chosen at f_{car}= 1.0 *kHz* or a higher value which satisfies IEEE standards for current THD. However, to achieve minimal THD levels, the PS-PWM method is necessary. In capacitive mode, when the STATCOM injects reactive power into the grid, the PS-PWM method should be preferred if no additional capacitor voltage balancing algorithm or control system is implemented. For both inductive and capacitive modes, the PS-PWM method is the most suitable option due to its operational advantages.

Table 6. Comparison of PWM methods based on suitability for various performance criteria

Performance criterion	Applicability degree		
	Low	**Medium**	**high**
Only semiconductor loss	PS-PWM	PD-PWM	POD-PWM APOD-PWM
Only capacitor voltage balancing	PD-PWM POD-PWM APOD-PWM	PS-PWM at f_{car}= 0.5 *kHz*	PS-PWM at f_{car}= 1.0 *kHz* and above
Only current harmonic content	PD-PWM POD-PWM APOD-PWM at f_{car}= 0.5 *kHz* for all	PD-PWM POD-PWM APOD-PWM at f_{car}= 1.0 *kHz* and above for all	PS-PWM
Only dynamic performance of dq current controllers	PD-PWM POD-PWM APOD-PWM	PS-PWM at f_{car}= 1.0 *kHz* and above	PS-PWM at f_{car}= 0.5 *kHz*

5. When all performance criteria are considered simultaneously, the POD or APOD-PWM method operating at a carrier frequency of f_{car}= 1.0 *kHz* can be recommended. Moreover, a voltage balancing algorithm or a switching signal swap method can be additionally used. This approach can minimize the semiconductor losses while solving the capacitor voltage imbalance problem. However, the additional control loop may slightly reduce the overall system reliability and cost.
6. Alternatively, the PS-PWM method operating at a low carrier frequency offers a simpler and more robust solution. To further suppress ripple voltages and improve voltage balancing, an auxiliary voltage balancing controller can also be integrated. The selection of the most appropriate PWM strategy should be guided by the practical design constraints, system reliability requirements, and the cost considerations.
7. Although increasing the carrier frequency in the PS-PWM method negatively affects the dynamic performance of the current controllers, the controllers still provide stable responses at all carrier frequency values. Therefore, relying solely on ISE and ITSE metrics may not be sufficient for the carrier frequency selection. Here, it is also important to consider the THD performance and the loss.

Comparative analysis reveals that no single PWM method satisfies all performance criteria simultaneously. In this respect, Table 6 summarizes the suitability of each PWM method with respect to the performance criteria.

CONCLUSION

This study has presented a comprehensive simulation-based evaluation of multiple carrier-based PWM schemes applied to an 11-level three-phase CHB-STATCOM operating at medium voltage. Four different modulation techniques, namely, PD-PWM, POD-PWM, APOD-PWM, and PS-PWM are comparatively assessed across four key performance criteria. These performance metrics are semiconductor losses, natural capacitor voltage balancing capability, harmonic distortion in the STATCOM current, and the dynamic performance of the decoupled dq current controllers. The results demonstrate that LS-PWM methods (PD, POD, and APOD) generally exhibit lower semiconductor losses which makes them attractive from an efficiency point of view. However, these methods are not advantageous in maintaining capacitor voltage balance. This problem is more severe under capacitive operating modes of the STATCOM. If LS-PWM methods are preferred auxiliary control methods or circuits to balance the capacitor voltages should be used. Among the level-shifted techniques, POD and APOD-PWM provides better performance than PD-PWM. However, for all of them the voltage ripples are unacceptable. In contrast, PS-PWM provides an effective natural capacitor voltage balancing and achieves acceptable THD levels. Even at relatively low carrier frequencies, PS-PWM generates harmonics which are compliant with IEEE Std 519. Furthermore, PS-PWM supports stable operation in both inductive and capacitive modes without any auxiliary balancing solutions. This can be a critical advantage in practical STATCOM applications. On the other hand, increasing the carrier frequency in PS-PWM will increase the switching losses. This problem can be worse particularly at relatively high carrier frequencies. Quantitative analysis with ISE and ITSE metrics indicates that a degradation in the dynamic performance of the current controllers can be observed when the switching frequency increases. The results show that, the PS-PWM method can be an effective semiconductor switching strategy when capacitor voltage balancing

and current harmonics are prioritized over efficiency. Alternatively, POD or APOD-PWM schemes may be considered if minimizing semiconductor losses is the primary design objective. However, in these approaches, additional voltage balancing control is required. The results obtained from this study can serve as a practical guideline for PWM selection in CHB-STATCOM systems.

DATA AVAILABILITY STATEMENT

The author confirms that the data that supports the findings of this study are available within the article. Raw data that support the finding of this study are available from the corresponding author, upon reasonable request.

CONFLICT OF INTEREST

The author declared no potential conflicts of interest with respect to the research, authorship, and/or publication of this article.

ETHICS

There are no ethical issues with the publication of this manuscript.

STATEMENT ON THE USE OF ARTIFICIAL INTELLIGENCE

Artificial intelligence was not used in the preparation of the article.

REFERENCES

[1] Sharma S, Gupta S, Zuhaib M, Bhuria V, Malik H, Almutairi A, et al. A comprehensive review on STATCOM: paradigm of modeling, control, stability, optimal location, integration, application, and installation. IEEE Access 2023;12:2701–2729. [CrossRef]

[2] Bamba S, Gupta SK. Enhancing power system stability through intelligent STATCOM control strategies in torsional oscillation environments. Sigma J Eng Nat Sci 2024;42:1933–1953.[CrossRef]

[3] Kannan A, Oliver S, Atallah A, Manchola AH, Aristi IA. Offshore wind farm grid integration: challenges and solutions for harmonic distortion. In: 23rd Wind & Solar Integration Workshop (WIW 2024); 2024 Oct. IET; 2024. p. 45–52.[CrossRef]

[4] Finotti C, Granata S, Borghetti G, Corsi G, Guarda F, Postiglione G, et al. 132-MVAr 35-kV STATCOM equipped with a novel power oscillation damping control strategy. IEEE J Emerg Sel Topics Power Electron 2025.[CrossRef]

[5] Yanmaz K, Altaş İH, Mengi OÖ. MFLC-PI controlled two level inverter based D-STATCOM for wind energy systems. Sigma J Eng Nat Sci 2017;8:161–168.

[6] Sanchez JH, Castro LM. Novel VSC-based STATCOM model based on dynamic phasors for unbalanced distribution networks. IEEE Open Access J Power Energy 2024;11:241–253.[CrossRef]

[7] Xu J, He G, Tang S, Gong Z, Wang C, Lan Y. The unbalanced control research of fractional-order cascaded H-bridge multilevel STATCOM. Fractal Fract 2025;9:30.[CrossRef]

[8] Li J, He Y, Liu J. Research on the capability of star-connected CHB-STATCOM to compensate the unbalanced voltage of power grid. IEEE Trans Power Electron 2025;40:8577–8591.[CrossRef]

[9] Demarcos A, Robles E, Ugalde U, Elosegui I, Andreu J. Output current ripple in electric vehicles with asymmetrical dual three-phase arrangement applying interleaved carrier-based PWM techniques. IEEE Access 2025;13:41743–41767.[CrossRef]

[10] Siva Prasad JS, Prasad KNV, Narayanan G. Experimental comparison of power conversion loss with different PWM strategies for STATCOM application. In: 2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020); 2020. IEEE; 2020. p. 1–6.[CrossRef]

[11] Benslimane A, Bouchnaif J, Essoufi M, Hajji B, Ldrissi LE. Comparative study of semiconductor power losses between CSI-based STATCOM and VSI-based STATCOM, both used for unbalance compensation. Prot Control Mod Power Syst 2020;5:1–14.[CrossRef]

[12] Gonzalez JO, Pérez-Estévez D, Wu R, Doval-Gandoy J, Mawby P, Alatise O. Power device losses in two-level converters with direct current controllers for grid-connected applications. In: 2021 IEEE Energy Conversion Congress and Exposition (ECCE); 2021. IEEE; 2021. p. 3154–3159.[CrossRef]

[13] Pereira HA, Cupertino AF, Xavier LS, Sangwongwanich A, Mathe L, Bongiorno M, et al. Capacitor voltage balance performance comparison of MMC-STATCOM using NLC and PS-PWM strategies during negative sequence current injection. In: 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe); 2016 Sep. IEEE; 2016. p. 1–9.[CrossRef]

[14] Melin PE, Guzman JI, Hernandez FA, Baier CR, Muñoz JA, Espinoza JR, et al. Analysis and control strategy for a current-source-based D-STATCOM towards minimum losses. Int J Electr Power Energy Syst 2020;116:105532.[CrossRef]

[15] Zhou J, Cheng PT. Modulation methods for 3L-NPC converter power loss management in STATCOM application. In: 2018 IEEE Energy Conversion Congress and Exposition (ECCE); 2018. IEEE; 2018. p. 3012–3018.[CrossRef]

[16] Sternberger R, Jovcic D. Theoretical framework for minimizing converter losses and harmonics in a multilevel STATCOM. IEEE Trans Power Deliv 2008;23:2376–2384.[CrossRef]

[17] Su YC, Cheng PT. Development of a hybrid cascaded converter based STATCOM with reduced switching losses and improved fault ride through capability. IEEE Trans Ind Appl 2020;57:3087–3096.[CrossRef]

[18] Tsolaridis G, Pereira HA, Cupertino AF, Teodorescu R, Bongiorno M. Losses and cost comparison of DS-HB and SD-FB MMC based large utility grade STATCOM. In: 2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC); 2016 Jun. IEEE; 2016. p. 1–6.[CrossRef]

[19] Liu Q, Rodriguez E, Farivar GG, Ceballos S, Townsend CD, Leyva R, et al. Discontinuous modulation of a cascaded H-bridge low-capacitance StatCom. IEEE Trans Power Electron 2021;37:2790–2800.[CrossRef]

[20] Hu K, Zhao G, Lu D, Lu Z, Xiang N, Wang S, et al. Simplified cluster voltage balancing control based on zero-sequence voltage injection for star-connected cascaded H-bridge STATCOM. CSEE J Power Energy Syst 2024;10:2255–2264.

[21] Oghorada O, Zhang L, Esan A, Egbune D, Uwagboe J. Inter-cluster voltage balancing control of modular multilevel cascaded converter under unbalanced grid voltage. J Mod Power Syst Clean Energy 2022;10:515–523.[CrossRef]

[22] Jin Y, Wang J, Xie B, Li L, Ji Y. A diode-clamped cascaded H-bridge STATCOM for voltage balancing of individual capacitors. Electr Power Syst Res 2018;163:452–460.[CrossRef]

[23] Khan JHH, Courteau G, Kissling S, Testa A, Foti S, Carpita M. Assessment of the star connected cascaded H-bridge to be used in STATCOM application. In: 2024 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM); 2024; Napoli, Italy. IEEE; 2024. p. 1136–1146.[CrossRef]

[24] Lu D, Wang J, Yao J, Wang S, Zhu J, Hu H, et al. Clustered voltage balancing mechanism and its control strategy for star-connected cascaded H-bridge STATCOM. IEEE Trans Ind Electron 2017;64:7623–7633.[CrossRef]

[25] Xu C, Chen J, Dai K. Carrier-phase-shifted rotation pulse-width-modulation scheme for dynamic active power balance of modules in cascaded H-bridge STATCOMs. Energies 2020;13:1052.[CrossRef]

[26] Sajadi R, Iman-Eini H, Bakhshizadeh MK, Neyshabouri Y, Farhangi S. Selective harmonic elimination technique with control of capacitive DC-link voltages in an asymmetric cascaded H-bridge inverter for STATCOM application. IEEE Trans Ind Electron 2018;65:8788–8796.[CrossRef]

[27] Hatano N, Ise T. Control scheme of cascaded H-bridge STATCOM using zero-sequence voltage and negative-sequence current. IEEE Trans Power Deliv 2010;25:543–550.[CrossRef]

[28] Barrena JA, Marroyo L, Vidal MAR, Apraiz JRT. Individual voltage balancing strategy for PWM cascaded H-bridge converter-based STATCOM. IEEE Trans Ind Electron 2008;55:21–29.[CrossRef]

[29] Vural AM. Self-capacitor voltage balancing method for optimally hybrid modulated cascaded H-bridge D-STATCOM. IET Power Electron 2016;9:2731–2740.[CrossRef]

[30] França JVG, do Carmo Mendonça D, Seleme SI, Pereira HA, Cupertino AF. On control of Delta-CHB STATCOM. IEEE Access 2025.[CrossRef]

[31] Reddy CL, Kumar PS, Sushama M. Performance comparison of star connected cascaded STATCOM using different PWM techniques. Int J Power Electron Drive Syst 2017;8:1303.[CrossRef]

[32] İnci M. Performance evaluation of multi-carrier PWM techniques: PD, POD and APOD. Int J Appl Math Electron Comput 2019;7:38–43.[CrossRef]

[33] S A, P R, Malegowda M, N C, B DGK. A comparative study of PD, POD and APOD PWM techniques with sinusoidal PWM reference signal on 5 level cascaded H bridge inverter. In: 2024 Asia Pacific Conference on Innovation in Technology (APCIT); 2024; Mysore, India. IEEE; 2024. p. 1–5.[CrossRef]

[34] Abdallah H, Yan X. Comparison of multicarrier PWM techniques for cascaded H-bridge multilevel inverter. Int J Power Electron Drive Syst 2017;8:861–868.[CrossRef]

[35] Maaroof HS, Al-Badrani H, Younis AT. Design and simulation of cascaded H-bridge 5-level inverter for grid connection system based on multi-carrier PWM technique. IOP Conf Ser Mater Sci Eng 2021;1152.[CrossRef]

[36] Reddy CL, Kumar PS, Sushama M. Design and performance analysis of cascaded H-bridge multilevel STATCOM. Int J Control Theory Appl 2017;10:1–11.

[37] Singh S, Agnihotri A, Bind S, Kumar S. Matlab simulation study and comparison of different multiple carrier PWM schemes for multi level CHB inverter. In: 2020 IEEE First International Conference on Smart Technologies for Power, Energy and Control (STPEC); 2020; Nagpur, India. IEEE; 2020. p. 1–6.[CrossRef]

[38] Sharma CK, Sathans. Comparative analysis of multi-carrier PWM methodologies for 3-phase 9-level cascade inverter. In: Proceedings of ICAEEC-2019; 2019 May 31-Jun 1; IIIT Allahabad, India. [CrossRef]

[39] O'Rourke CJ, Qasim MM, Overlin MR, Kirtley JL. A geometric interpretation of reference frames and transformations: dq0, Clarke, and Park. IEEE Trans Energy Convers 2019;34:2070–2083.[CrossRef]

[40] Carrara G, Gardella S, Marchesoni M, Salutari R, Sciutto G. A new multilevel PWM method: a theoretical analysis. IEEE Trans Power Electron 1992;7:497–505.[CrossRef]

[41] Infineon Technologies. 6500V/250A FD250R65KE3-K IGBT module datasheet. Available at: https://www.infineon.com/assets/row/public/documents/24/49/infineon-fd250r65ke3-k-datasheet-en.pdf. Accessed November 10, 2026.