



## Research Article

# Energy-efficient static memory architecture for internet of things applications

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## ABSTRACT

The paper explores low-power design strategies of Static Random Access Memorycell for Internet of Things devices to address critical power limitations that hinder further miniaturization. Fin-Field Effect Transistor solves the problem of leakage current by improving challenging power versus performance decision. This research develops 7-Transistor Static Random Access Memorycells based on Fin-Field Effect Transistors using the Muti-Threshold CMOS and Self Controllable Voltage Level methods. Using 45 nm Fin-Field Effect Transistor technologies, the design and simulation of all design circuits are carried out with Cadence Virtuoso. The work adopts a multi-disciplinary approach, combining device-circuit co-design to achieve ultra-low-power operations suitable for complex tasks in Internet of Things based systems. The proposed design shows that the Self Controllable Voltage Level approach of a 7-Transistor Static Random Access Memory design utilizing Fin-Field Effect Transistor cell is more effective than the Muti-Threshold CMOS methodology in terms of leakage power and leakage current. Additionally, among other proposed approaches, a comparative analysis of leakage currents and leakage power is conducted. Key outcomes include significant improvements in leakage power using Self Controllable Voltage Level approach for Static Random Access Memory design using Fin-Field Effect Transistor. This paper contributes to the advancement of low leakage Internet of Things devices by integrating innovative leakage reduction techniques with cutting-edge low-power circuit designs. The proposed design achieves a minimum leakage current of 9.45nA and leakage power of 24.28nW by utilizing Self Controllable Voltage Level approach. Compared to Static Random Access Memorycells designed with Muti-Threshold CMOS technique, the proposed method results in 25.8% and 36% approximately reduction in leakage power and leakage current respectively. The findings pave the way for developing smaller, smarter, and sustainable wearable and implantable devices capable of complex tasks without reliance on batteries.

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## INTRODUCTION

A significant challenge in modern circuit design is reducing power consumption in electronic components. In existing chip technology, the capacity of SOC memory is rapidly advancing to enhance global performance. As a larger backup memory is necessary, SRAM plays an increasingly vital role in contemporary chip systems [1]. With shrinking transistors, reliability problems like SCEs and process variations are getting more and more critical. Moreover, if the current density is high in silicon, heat dissipation is also a problem, which is also detrimental to the durability and operation life of circuits.

As the number of IoT devices increases, memory technologies must be power efficient, fast and space efficient. The IoT is gaining popularity in fields such as home automation systems, biomedical equipment, and wearable communication devices. IoT-compatible devices require larger integrated memory circuits. Compact and light-weight IoT devices restrict the utilization of the major energy source to diminutive non-rechargeable or rechargeable batteries. Battery longevity and replacement intervals are key concerns in battery-operated or partially energy-harvested IoT devices, ultra-low-power (ULP) systems on chips (SoCs) are increasingly favored by chip manufacturers. This ULP system on chips necessitates that both the logic and the embedded SRAM within the processor function at extremely low supply voltages. The IoT is now playing a significant role in the electronics sector and is in great demand. The industrial IoT market can be expected to be driven by applications like industrial automation and predictive maintenance, which are expected to reach as big as \$263.4 billion by 2027 [2]. In 2025, the World Economic Forum estimates that there will be 41.6 billion connected devices [3]. For diverse tasks, on-chip memory is needed for storing instructions, and the required memory is SRAM for IoT devices [4, 5]. These recollections use up a large amount of the system's energy [6]. SRAM leakage power may govern total chip  $P_{\text{Leakage}}$ , and substantial switching capacitance in the bit lines and word lines enables SRAM access operations energy-intensive. Operating the SRAM capacitance in the bit lines and word lines enables SRAM access operations energy-intensive. Operating the SRAM at the sub-threshold region minimizes  $P_{\text{Leakage}}$ , rendering it appropriate for low-power applications. SCEs due to continuous scaling also impact the performance of CMOS-based SRAM [7]. Alternative devices like FinFET have been created to address the constraints of CMOS technology. A FinFET is a structure with a channel that is surrounded by the gate material on three or more sides, which offers better control and improved performance compared to a CMOS device. The advantages of FinFET devices over conventional CMOS devices are scalability and on-current [2, 8]. However, the important problem of width quantization arises in circuits using FinFETs [9] exists. This is a major concern for radioed circuits like SRAM, where the

size of the transistors is critical to the proper functioning of the circuit. This is further complicated by inconsistencies in the manufacturing process, and results in a lowered efficiency of the SRAM design. An innovative gadget capable of addressing these restrictions is essential at this time.

Currently, Nobel multi (tri)-gate structural design, commonly referred to as FinFET technology, has demonstrated enhanced scalability. The primary factor influencing the IC industry include cost, time to market, area, power consumption, and performance metrics. The design specifications have remained consistent over time. With every new process node, design teams try to make their products "better, sooner, cheaper." These days, processors are built with billions of transistors. The industry shift to smaller geometries could pose problems because of the effects of short-channel (SCE) which may lead to increased leakage current with reduced geometry and variation in the concentration of dopants with decreasing geometry. The FinFET structure offers substantial benefits for the ability to scale devices and reduce short channel effects, which are common in many contemporary planar transistor designs, in the future semiconductor industry. Estimations [10, 11] show that the FinFETs can reach an operational speed that is up to 37% higher and require less than half of the dynamic power, while simultaneously consuming less static leakage current.

The FinFET exhibit has improved speed, but at roughly the same power, or has similar speed with lower power, when compared to its planar counterpart. Design teams will be able to now design for power, performance and throughput to meet the needs of particular utilities. As a result, multi gates FETs are anticipated to contribute to the reduction of leakage and the scaling of gate length. The advantages of FinFET are that it is scalable without any arbitrary dopant fluctuation effects, has higher channel mobility, and can be used to realize the next generation of SRAM with enhanced scalability with respect to gate insulator thickness. SRAM cells with FinFET technology can achieve smaller area and lower leakage currents. The threshold voltage ( $V_{\text{TH}}$ ) of the access transistor can be dynamically changed to improve data stability. While FinFETs can mitigate  $V_{\text{TH}}$  variation, there are many challenges to reduce the variation. The small sizes of memory storage units allow for high storage density while maintaining performance and reliability. SRAM functions without the requirement for data refresh cycles, which makes it faster than other types of memory and increases the amount of data that can be stored, due to its internal positive feedback mechanism. SRAM cells are becoming more popular because they are more efficient, leading to greater data retention and larger write voltage range with the minimal power supply voltages. Table 1 illustrates the comparative study of earlier designed SRAM using FinFET [12-21].

Several low-power methods, including power gating, MTCMOS, SVL, VTCMOS and stacking can lower leakage current and power dissipation [22-24]. Initially, traditional

**Table 1.** Comparison of FinFET based SRAM design

| S. No. | Pub. Year | Ref. No. | Authors Name                | Transistors Count | Power Consumption                                                                       | Propagation Delay                                                          | Power Delay Product                                                       |
|--------|-----------|----------|-----------------------------|-------------------|-----------------------------------------------------------------------------------------|----------------------------------------------------------------------------|---------------------------------------------------------------------------|
| 1      | 2021      | [12]     | Raushan et al.              | 12                | 99% more efficient than traditional SRAM                                                | 79.2% more efficient as compare to traditional SRAM                        | 99.7% more efficient as compare to traditional SRAM                       |
|        |           |          | Raushan et al.              | 14                | 99% more efficient than traditional SRAM                                                | 76.5% more efficient as compare to traditional SRAM                        | 99.4% more efficient as compare to traditional SRAM                       |
| 2      | 2020      | [13]     | Rahebeh Niaraki Asli et al. | 6                 | Least read power consumption                                                            | NA                                                                         | NA                                                                        |
| 3      | 2020      | [14]     | S. Birla et al.             | 8                 | At 0.5 V, the SG and IG SRAMs had leakage powers of 12.61 nW and 8.92 nW, respectively. | NA                                                                         | NA                                                                        |
| 4      | 2020      | [15]     | C.Duari et al.              | 8                 | At 0.5 V, leakage power is 5.63nW for CMOS SRAM.                                        | NA                                                                         | NA                                                                        |
| 5      | 2020      | [16]     | R. R. Vallabhuni et al.     | 7                 | At $V_{DD}=0.1\text{v}$ , 0.001224mW for write operation.                               | At $V_{DD}=0.1\text{v}$ , the write operations take 0.2943 ns.             | At $V_{DD}=0.1\text{v}$ , the write operations take 0.003602 pJ.          |
| 6      | 2019      | [17]     | J.Verma et al.              | 8                 | 0.0268 $\mu$ W for writing operation.                                                   | 0.0383 ns for writing operation.                                           | 0.001026 fJ for writing operation.                                        |
| 7      | 2018      | [18]     | S. S. Ensan,et al.          | 11                | 5.17 nW and 137.66 nW, respectively, represent the static and average power.            | 230.46 ps & 491.8ps delay for write and read operation respectively.       | 168.57 aJ                                                                 |
| 8      | 2016      | [19]     | J.Verma et al.              | 13                | Leakage power = 0.096 nW                                                                | 7.8 ns                                                                     | 0.7488 fJ                                                                 |
| 9      | 2016      | [20]     | N. Kaur,et al.              | 10                | 138.82 nW and 24.52 nW for writing and reading operation respectively.                  | 60.069 ns and 0.00024056ns for writing and reading operation respectively. | 1.4442 aJ and 0.0058986aJ for writing and reading operation respectively. |
| 10     | 2015      | [21]     | D.Verma et al.              | 6                 | 1.709 $\mu$ W for reading and 7.561 nW for writing operation.                           | 21.44 ns & 20.55 ns for reading and writing operations respectively.       | NA                                                                        |

CMOS was used in SRAM design. However, this results in issues such as increased  $I_{\text{leakage}}$  and elevated power dissipation, which reduce the functionality of SRAM. Reducing power dissipation, achieving faster access times, and minimizing  $I_{\text{leakage}}$  are key requirements for memory design [25]. Hence, SRAM cells using FinFETs are recommended over conventional or traditional SRAM cells. Compared with traditional SRAM design architectures, FinFET technology minimizes SCE [26].

Additionally, reducing the leakage characteristics of SRAM cells is essential for improving cell stability [27]. The capability of FinFETs to differentially bias the independent

front and back gates, which permits control over the device's  $V_{\text{TH}}$  and current, is one of its most beneficial characteristics. By adjusting the back gate, FinFETs can further minimize the power consumption of SRAM cells [28]. This section also addresses some research gaps in current methods for improving the design of FinFET based SRAM cells.

- **Less Extent of Novelty:** An obstacle to future progress is the fact that most research on enhancing the performance of SRAM cells focuses on either changing the number of transistors or using FinFET devices of varying sizes.

- **Less Studies toward Optimization:** An optimization model must be developed in order to address the fault tolerance concerns and enhance the SRAM FinFET design performance. Mathematical optimization techniques backed by probability theory are needed to enhance the design concepts of SRAM-based FinFETs.
- **Less number of computational Modeling:** The majority of current methods for FinFET-based SRAM rely on hardware-based modeling environments or experimental methods. Although experimental approaches provide highly reliable results, their application for large-scale, real-time commercial use is limited due to the lack of thorough consideration of computational complexity. On the other hand, hardware-based methods rely on specific simulation environments, which limit the amount of computational power that can be utilized.

To address these challenges, ICs, the primary power-consuming components of IoT devices, are designed to operate in low-power modes by reducing the supply voltage using low-voltage design approaches. The importance of low power memory cells for IoT applications are shown in Figure 1 and mentioned below:

- **Maintenance savings and increased reliability:** A low power consumption of the memory directly equates to a longer operational life of battery-powered systems, which is beneficial in the fields of environmental monitoring, smart agriculture and industrial automation, among others.
- **Energy Harvesting Compatibility:** There are many modern IoT nodes that depend on energy harvesting (solar, thermal, RF, etc.) for power. This is because a feature of these devices is that they can operate with very restricted energy budgets, thanks to their low-power memory cells.
- **Thermal Management:** Reducing power consumption reduces thermal dissipation, especially important for small IoT devices with little heat dissipation capacity, ensuring long-term reliability and decreased cooling costs.

- **Always-On Operation:** IoT devices may require memory cells to store data when they are inactive or sleeping. Ultra-low leakage memory designs are capable of providing always-on features without consuming energy, while providing responsive real-time performance and wake-up security.
- **Edge Intelligence Enablement:** As edge computing and on-device processing gain more importance, memory is critical to enable local inference, decision making and data filtering for edge Intelligence Enablement. Efficient memory design improves the computational power while keeping the energy efficiency.
- **Scalability and Network Density:** Power efficiency per node enables the use of more nodes without increasing the energy consumption, thus, leading to better scalability and network density for large-scale IOT networks deployed in smart cities, logistics and health monitoring systems.

This paper contributes to the advancement of low leakage IoT devices by integrating innovative leakage reduction techniques with cutting-edge low-power circuit designs. The proposed design achieves a minimum leakage current of 9.45nA and leakage power of 24.28nW by utilizing SVL approach. Compared to SRAM cells designed with MTCMOS technique, the proposed method results in 25.8% and 36% approximately reduction in leakage power and leakage current respectively. The subsequent sections of the paper are structured as follows. Discuss about Structure of the FinFET in Section 2, discuss about the Static Random Access Memory cell in Section 3, describe the SRAM Design Challenges in Section 4, Section 5 explains the Energy-Efficient SRAM Design approach; Section 6 discuss about the results. Section 7 gives the conclusions and prospective research directions.

## FINFET STRUCTURE

The term FinFET was originally invented by the University of California. It was predominantly a

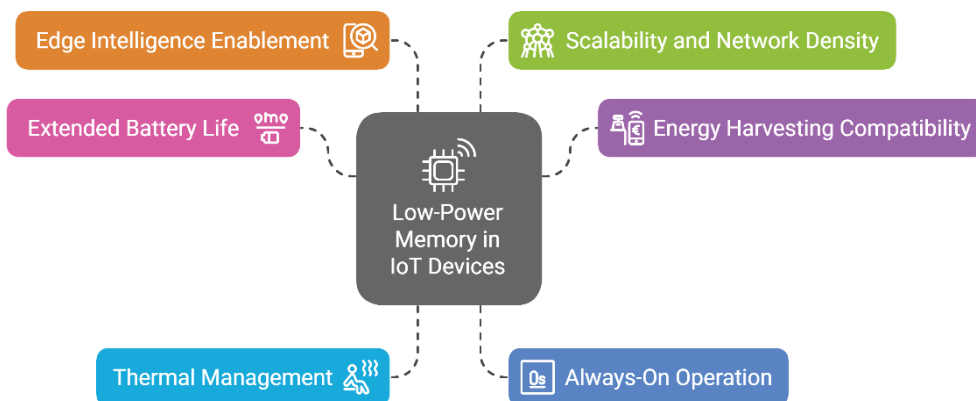


**Figure 1.** Benefits of Low-Power Memory in IoTDevice.

non-planetary transistor, featuring two gates fabricated on the SOI, designed as part of the DELTA, specifically a single-gate pre-transistor. FinFET comprises dual gates, whereas planar MOSFET contains a single gate to regulate the channel and encompasses the source and drain [29]. FinFETs, a variant of multi-gate FET (MGFET), are predicted as one of the highly promising alternatives to bulk MOSFETs. Their potential is attributed to their superior stability, enhanced ( $I_{ON}/I_{OFF}$ ) ratio, improved short channel performance, and reduced intrinsic gate capacitance. The operational methodology of FinFET closely resembles that of conventional MOSFET. FinFETs possess gate, drain, and source terminals to control the current flow. The channel between the source and drain of a FinFET is the distinguishing feature that sets it apart from a MOSFET. A “Fin” is a three-dimensional structure resembling the FinFET channel located on the upper section of the silicon substrate. Figure 2 illustrates that the three-dimensional bar design entirely encases the FinFET gate around the channel, creating multiple gate electrodes on both sides. These electrodes may enhance driving current and reduce leakage effects. The fin height of a single-fin FinFET should be half of the effective channel width ( $W_{eff}$ ), as per the design specifications [30]. Conversely, FinFETs can provide greater driving current densities per unit area than planar devices, provided that the effective width ( $W_{eff}$ ) is adequate to accommodate multiple parallel fins. The primary distinctions between FinFET and MOSFET devices lie in the configuration of the channel within the plane and the number of gates present. FinFET features a vertical channel referred to as ‘Fin’, whereas planar MOSFETs possess a horizontal channel, as indicated in references [31]. The fin structure quantifies the channel width based on the fin length. The result of this calculation is subsequently multiplied by the end height and the fin width within the Triple-Gate Multigate-transistor configuration. Consequently, the enhancement of cases is proportional to the quantity of gates and the iterative development of wings. The current drive may be enhancing due

to longer fin lengths, but this improvement could compromise the stability of the machinery [32]. The  $W_{eff}$  of FinFET is given by eq. (1) [33].

$$W_{eff} = N_{Fin} \times (T_{Fin} + 2H_{Fin}) \quad (1)$$

The FinFET architecture features a thin, vertically oriented, fin-shaped channel that facilitates current flow and is encased by a gate responsible for regulating electron movement. The vertical architecture facilitates enhanced management of electron flow in comparison to conventional planar MOSFETs, resulting in superior performance and efficiency. The DG FinFET is classified as a single-gate structure due to the width of the fin ( $W_{Fin}$ ) is being considerably greater than its height ( $H_{Fin}$ ) and the gate oxides on the sidewalls being substantially thicker than those on the top. Silicon dioxide and high-k dielectrics are commonly used as gate dielectrics due to their properties. High-k dielectrics, in particular, possess elevated dielectric constants that minimize gate leakage current. Spacer materials are used for forming a gap between the source/drain region and the gate electrode. The width of the gate and length of the channel are controlled by the size of the spacers and thus the performance characteristics of the transistor.

#### Static Random Access Memory Cell

An SRAM is a type of volatile semiconductor memory that is often used in digital systems for fast storage and retrieval of data. SRAM stores the data permanently, i.e. without refresh cycles as long as the power supply. This is because each bit in the SRAM is stored in a bistable flip-flop circuit. These transistors create a latch which allows the bit to stay in one state, which gives certain applications SRAM faster and more reliable. This memory is organized in the form of an array, making it easy to access bits and giving it design flexibility. Upon verification of the functionality of an individual memory cell array, it can be duplicated numerous times with little modification to the I/O control circuitry. The general architecture of SRAM design

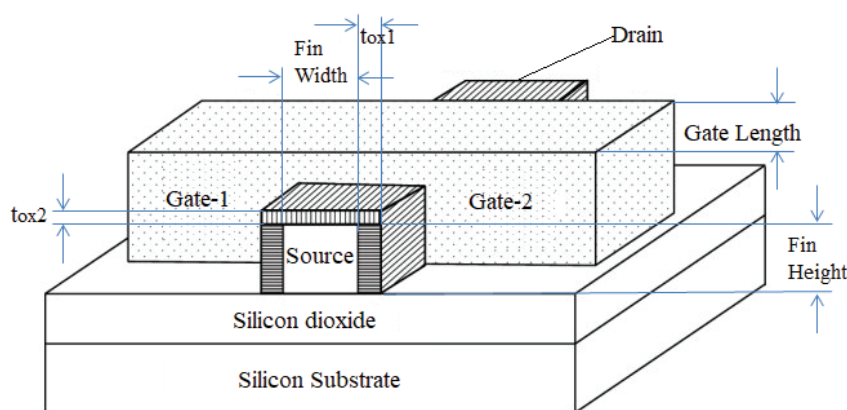


**Figure 2.** FinFET Structure.

is represented in Figure 3. The operational state of SRAM concerns to its functionality during various phases, including read, write, and stand by modes.

Figure 4 illustrates a 7T SRAM cell utilizing FinFET technology. This SRAM cell comprises a total of seven transistors: five N-type and two P-type FinFETs. The SRAM cell presented uses double-cross-coupled inverters and double-access transistors, both constructed with FinFET devices. The SRAM design consists of two sets of cross-coupled inverters, utilizing four transistors (M1, M2, M3, and M4), with each bit stored across these transistors. The 7T SRAM cell, which utilizes FinFET technology, effectively addresses the leakage issue present in the 6T SRAM cell.

This proposed design incorporates a total of seven transistors. Four transistors work like those in a standard device, while the other transistor controls the device so that in read mode, M6 and M5 are turned ON and M7 is turned OFF; on the other hand, in write mode, M5 is turned off, which helps save power.

**Write Operation:** The write operation of an SRAM design utilizing FinFET technology depends on the feedback connection established between the cross-coupled inverters. In this single-transistor-pair method, data increases and decreases as a function of the ON/OFF state of M2. Setting the bit line and the RL line simultaneously initiates the reading process. This procedure takes place when the word line is retained by access transistors M7 and M6.

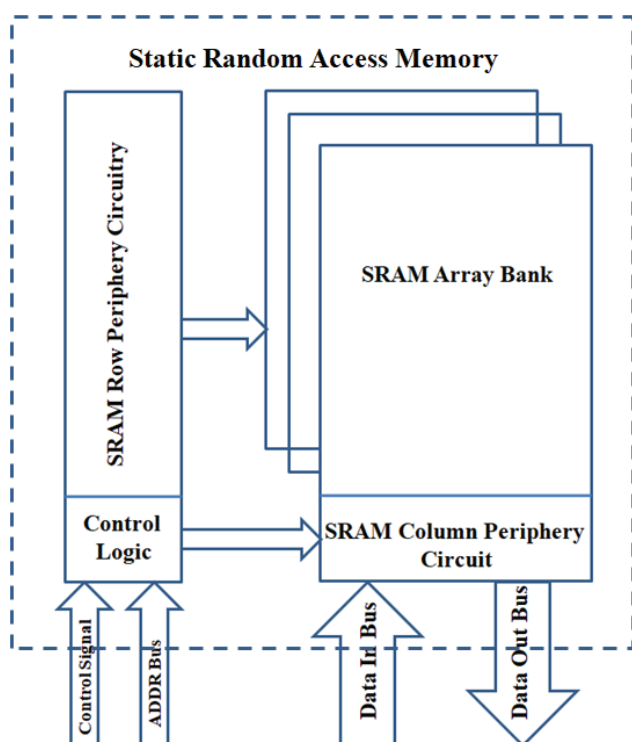


Figure 3. SRAM architecture.

**Read Operation:** Here, information data is transmitted to the bit line as well as the word line. The data assigned to both lines is complementary to one another. The data is stored once the word line is stimulated. Improving FinFETs count of fingers can improve the operation write, but this improvement won't happen in all situations [34].

**Hold Operation:** Transistors M3 and M4 function as OFF-inverter transistors, providing mutual support to maintain data for an extended period. In this state, there is no connectivity between the RL, WL, and bit line with the cross-coupled circuit [35].

In SRAM, the hold state denotes the condition in which data is preserved without being accessed or change. SRAM cells generally consist of six transistors; however, certain designs incorporate seven transistors to improve stability or minimize leakage currents. In an alternative operating mode, the power consumption of suggested SRAM is decreased to 50% of that of a typical circuit, since it utilizes only one bit line [36].

Figure 5a displays the 7T SRAM design simulated write waveform result. We have carried out a single-ended procedure. At BL node, a pulsed input is applied and output is measured from Q and  $\bar{Q}$ . For this operation, WL is maintained at HIGH and RL at LOW. Figure 5b displays the 7T SRAM design simulated read waveform result. At Q node, a pulsed input is applied and output is measured at BL. For this operation, WL is maintained at LOW and RL at HIGH [37].

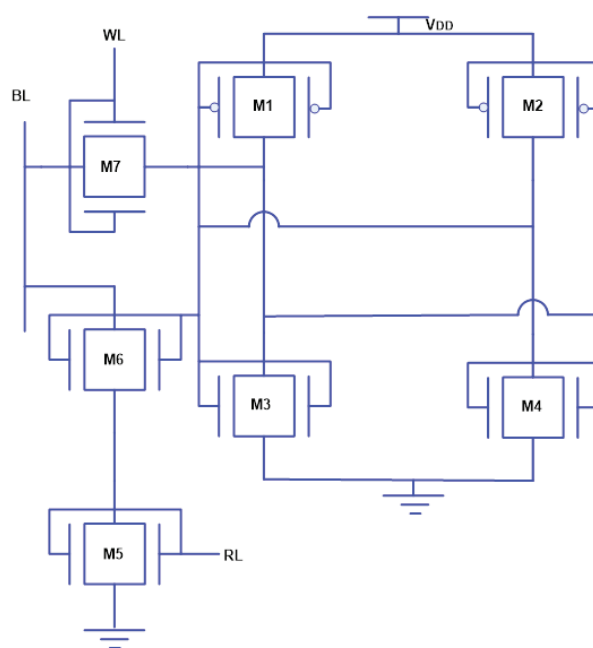
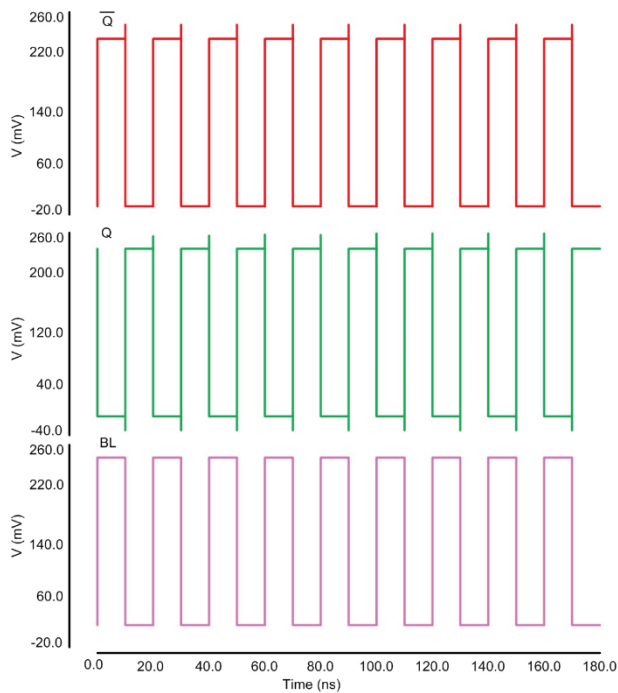
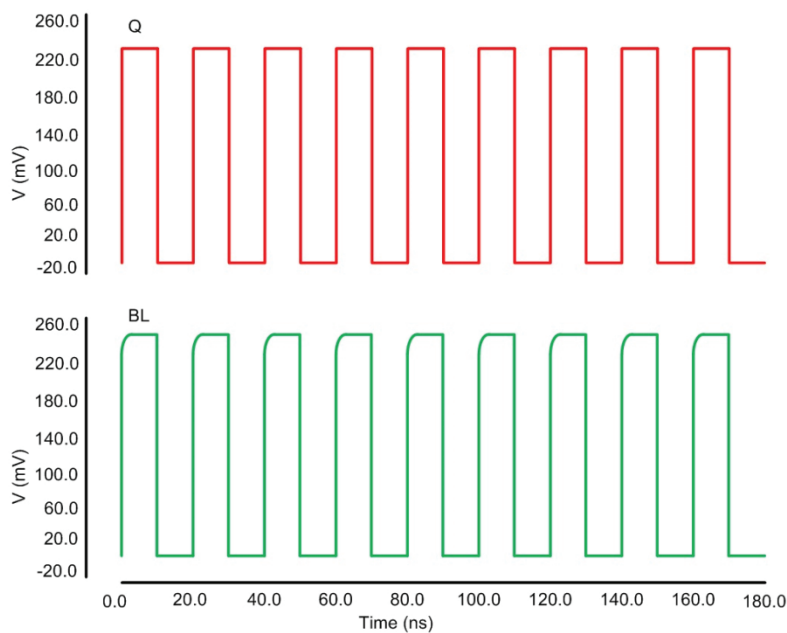


Figure 4. 7T SRAM cell using FinFET technology.



(a)



(b)

**Figure 5.** Operations of 7T SRAM using FinFET technology: (a) Write (b) Read.

### SRAM Design Challenges for IoT

Designing SRAM for IoT applications presents several unique challenges, primarily due to the stringent requirements of IoT devices. These challenges include:

- **Power Consumption Constraints:** One of the primary challenges in designing SRAM for IoT applications is minimizing power consumption. Most IoT devices
- **Area and Cost Efficiency:** IoT devices are highly area-constrained due to their small form factors. SRAM

operate on battery power or energy harvesting systems, making ultra-low power design a necessity. SRAM typically consumes more static power compared to other memory types due to leakage currents, especially as technology scales down to sub-10nm nodes.

- **Area and Cost Efficiency:** IoT devices are highly area-constrained due to their small form factors. SRAM

cells must be extremely compact while maintaining functionality and reliability. Designers face the challenge of reducing the cell size without sacrificing performance or yield.

- **Variability and Process Scaling:** Process variations (e.g., threshold voltage, line-edge roughness) become more prominent in scaled CMOS technologies, which directly impact the reliability and performance of SRAM cells.
- **Low Voltage Operation:** IoT devices often run at reduced supply voltages to save power, but this significantly affects the read/write stability and noise margins of SRAM cells.
- **Reliability and Data Retention:** SRAM must retain data reliably, especially for devices in sleep modes or intermittent connectivity, which is common in IoT scenarios. Long idle times can exacerbate data retention issues and bit flipping due to leakage or soft errors.
- **Security and Data Privacy:** In many IoT applications (e.g., healthcare, smart homes), SRAM may store sensitive data. Designers must account for physical attacks or side-channel attacks targeting memory.
- **Integration with Heterogeneous Systems:** IoT systems integrate multiple types of logic, analog, RF and sensor interfaces. SRAMs need to work in mixed-signal environments and be fabricated inside SOCs with different requirements.
- **Scalability:** Design must be scalable to accommodate a range of applications from wearable devices to implantable systems without significant re-engineering. Therefore, the scaling of the CMOS technology is reaching some limits and other technologies are being investigated, such as FinFETs, tunnel FETs (TFETs) [38] and carbon nano-tube transistors (CNTs). Of these, FinFET technology has emerged as the most viable alternative to CMOS.

- **AI and IoT Integration:** Many biomedical devices are now part of IoT systems or use AI for diagnostics. SRAM needs to efficiently support these data intensive operations and hence needs to be optimized for both computational and storage requirements [39].

Innovations such as new transistor architectures, FinFET, advanced error-resilience techniques and energy-efficient design methodologies are exploited to overcome these challenges and to meet the demanding requirements of portable devices. The challenges in designing SRAM for IoT applications are shown in Figure 6.

### Design Approach for Energy-Efficient SRAM

#### Multi-threshold cmos approach

The Multi-threshold CMOS approach has emerged as a key enabler for low power design in modern ICs. It smartly exploits the transistors with different threshold voltages to efficiently overcome the problem of leakage power while fulfilling the required performance [40]. Despite some design and implementation issues, its advantages make it an integral part of low power design methodologies. Future advances in automation, AI based design and combination with other power saving techniques is likely to improve the efficacy and adoption of Multi-Vt CMOS. As technology is scaled down issues like power consumption and leakage currents are becoming more important. Here, the Multi-Vt CMOS design has emerged as a powerful technique to achieve the trade-off between high performance and low power consumption, particularly in battery operated and energy constrained devices like mobile phones, portable electronics, and IoT systems.

The basic concept of the Multi-Vt CMOS methodology is to integrate transistors with different threshold voltages ( $V_{TH}$ ) in a single IC. The  $V_{TH}$  of a MOSFET is defined as the minimum gate voltage required creating a conductive path

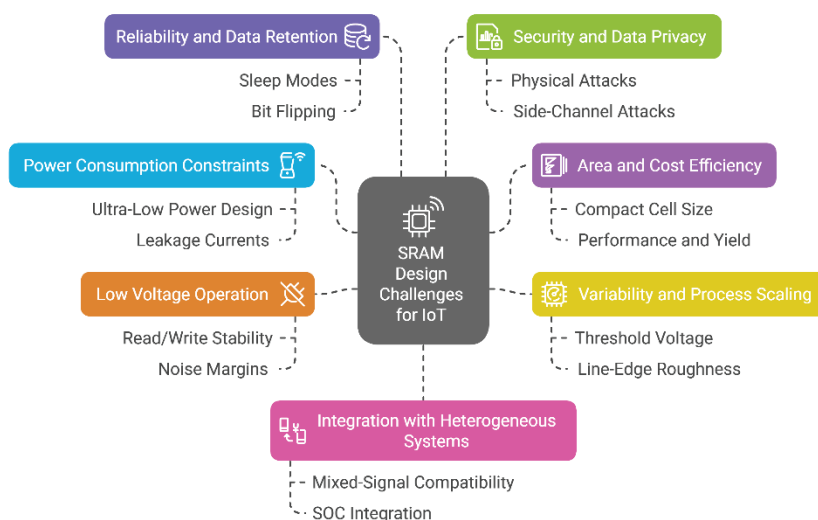


**Figure 6.** Challenges in designing SRAM for IoTDevice.

between the sources and draining terminals. Reducing the threshold voltage improves the switching speed of the transistor which in turn improves the performance. However, this also results in an exponential increase of subthreshold  $I_{leakage}$  that is a major contributor to static power dissipation in particular for idle or standby mode. In contrast, transistors with higher threshold voltage will have lower leakage current, but will switch slower. This could affect the performance. Multi-Vt CMOS design exploits this trade-off by using LVT (low-Vt) transistors on timing-critical paths for high-speed operation and HVT (high-Vt) transistors on non-critical paths where some loss of performance is acceptable in return for less leakage power. This method allows designers to optimize circuits for both dynamic and static power consumption without drastically affecting overall performance. The implementation through the MTCMOS approach involves leakage power reduction by utilizing transistors that operate in sleep mode. These associated transistors are activated in ON mode and deactivated in OFF (Sleepy) mode via a clock/sleep signal. A Transistor in Sleepy mode significantly decreases static leakage current when the SRAM is in the off condition. Figure 7 illustrates the proposed 7-T based SRAM cell, which is developed utilizing the MTCMOS approach.

When sleep transistors are turned OFF,  $V_{DD}$  and ground are automatically cut off from the SRAM cell, which lets data bits 0 and 1 exist on either side of the SRAM, effectively creating virtual power rails. In the MTCMOS method, multiple

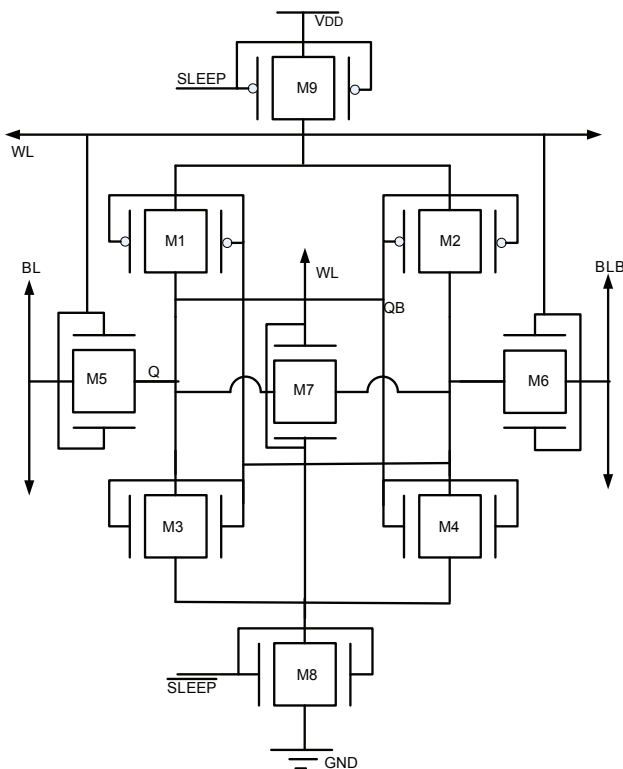


**Figure 7.** 7T SRAM design using MTCMOS approach.

threshold voltages are applied to different transistors based on their role and the requirements of the circuit, allowing for a better balance between power, performance, and area (PPA).

### Self controllable voltage level (SVL) approach

The SVL approach is a power reduction way used in VLSI design to reduce leakage power, particularly in low-power applications such as portable and battery-operated devices. This approach is also known as dynamic voltage and frequency scaling (DVFS). The key idea of SVL is to dynamically control the supply voltage of a circuit block based on its operational state. This approach might imply a method where a system autonomously manages its own voltage level. This approach may incorporate self-regulation mechanisms, maybe via internal sensors or feedback loops, enabling the system to dynamically alter its voltage level according to its operating conditions. The developed SRAM operates in two modes: active mode and standby mode.

- When a circuit is active, it operates at the normal supply voltage to maintain performance.
- When a circuit is idle or in standby mode, the SVL approach either raises the ground potential (virtual ground) or lowers the supply voltage (virtual  $V_{DD}$ ), effectively reducing the voltage across the transistors. This drastically reduces subthreshold leakage currents, which are a major component of static power consumption in modern CMOS technologies.

The SVL helps in retaining the data retention by offering finer control through modulating the voltage levels, compared to completely disabling the circuit blocks as done by the traditional power gating techniques. This is usually done by using specially designed control transistors or circuits that sense the state of the logic block and adjust the supply or ground levels accordingly. SVL is very useful when the design needs to switch between active and idle states often and provides good tradeoff between saving leakage power and wake-up time.

There are a few major advantages of the SVL circuit. In the SRAM active mode, the ON switch feeds the on MOS with the peak  $V_d$ , resulting in a fast operation of the SRAM circuit. In standby mode the SRAM drives the MOS transistor with slightly increased  $V_s$ , while a “weakly on switch” reduces  $V_d$ . This provides a high noise immunity of the SVL circuit. The decrease in the standby power is attributed to the increase in  $V_{TH}$  and the reduction in the subthreshold current ( $I_{sub}$ ) of the “off MOS” transistor [41].

### Advantages of SVL approach

This approach presents several benefits compared to alternative leakage current reduction strategies, including:

- Significant Leakage Reduction: SVL effectively reduces subthreshold leakage by stacking transistors and elevating the virtual ground or supply, minimizing leakage during standby mode.
- Low Area Overhead: Compared to other methods like MTCMOS (Multi-Threshold CMOS), SVL generally

introduces lower layout area overhead, making it suitable for compact designs.

- iii. No State Loss During Standby: Unlike power gating, SVL maintains the internal state of the circuit in sleep mode, eliminating the need for data retention strategies.
- iv. Faster Wake-Up Time: Since the circuit remains partially powered, SVL allows quicker recovery from sleep mode compared to approaches that fully cut off power.
- v. Simplified Control Logic: The control mechanism for SVL is relatively straightforward, reducing design complexity and power management circuit requirements.
- vi. Better Suitability for Low-Voltage Designs: SVL is particularly effective in ultra-low voltage designs, where other approaches may struggle with performance or stability.
- vii. Reduced Need for High-V<sub>th</sub> Devices: Unlike MTCMOS, which relies heavily on high-threshold devices (with higher delay), SVL can use standard-V<sub>th</sub> transistors while still achieving leakage savings.

#### 7T SRAM design using upper SVL-approach

Figure 8 illustrates the SRAM cell utilizing FinFET with the USVL approach. The USVL circuit consists of double n-channel-type FinFET transistors (resistors) arranged in series with a single p-channel-type FinFET transistor (switch). The USVL circuit is connected with upper side of 7T SRAM cell and CS signal is used as a controlling signal. The ON P-channel type transistor is connected to  $V_{DD}$  and the 7T SRAM cell utilizing FinFET in active mode upon request. Similarly, the ON N-channel type transistor is

connected to  $V_{DD}$  and the 7T SRAM cell employing FinFET in standby mode. This approach entails the application of the full supply voltage ( $V_{DD}$ ) to the 7T SRAM design during active mode, while reducing the voltage level ( $V_D$ ) during standby mode (sleep mode).

Simulation results show that using a lower gate voltage on transistor FinFET M6 reduces the unwanted current that leaks through the device. The decrease in FinFET M3 channel voltage leads to a reduction in gate leakage current, which in turn results in a lower gate channel voltage across M4. The leakage gate current of M1 is consistent and shows no variation. The USVL circuit-based P-channel FinFET M8 exhibits little leakage current. The leakage current stays uniform across M1, but the USVL method diminishes the sub-threshold leakage current via transistors M2 and M3. The gate leakage currents in access FinFETs M7 and M6 stay constant in this approach. The suggested SRAM utilizing USVL exhibits a leakage power of 26.98 nW, exceeding 10% compared to hybrid SVL approach. In summary, two components of gate leakage current in access transistors remain the same despite the USVL approach enhanced efficacy in reducing leakage gate current. Furthermore, it generates an additional subthreshold  $I_{leakage}$  in the access transistor while preserving one subthreshold current component within it [42].

#### 7T SRAM design using lower SVL approach

Figure 9 illustrates the SRAM cell that incorporates FinFET technology utilizing the USVL approach. The Lower SVL circuit consists of two p-channel type FinFET

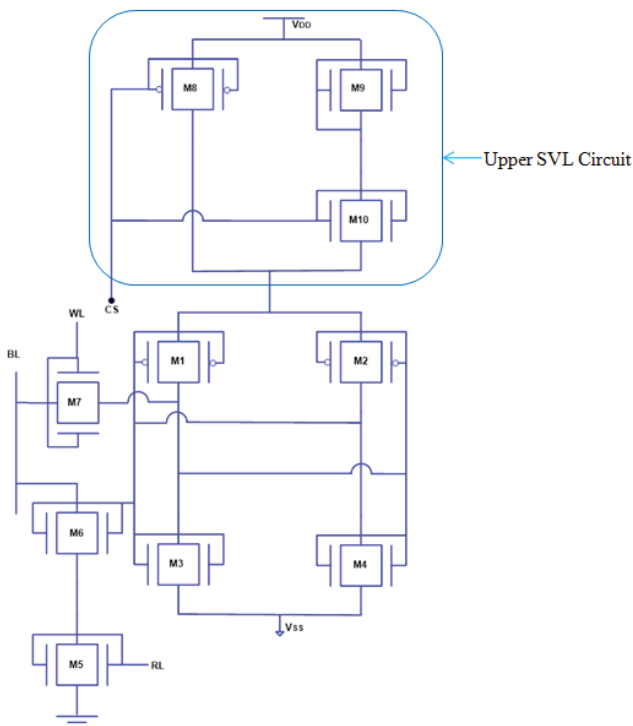


Figure 8. 7T SRAM cell with USVL approach.

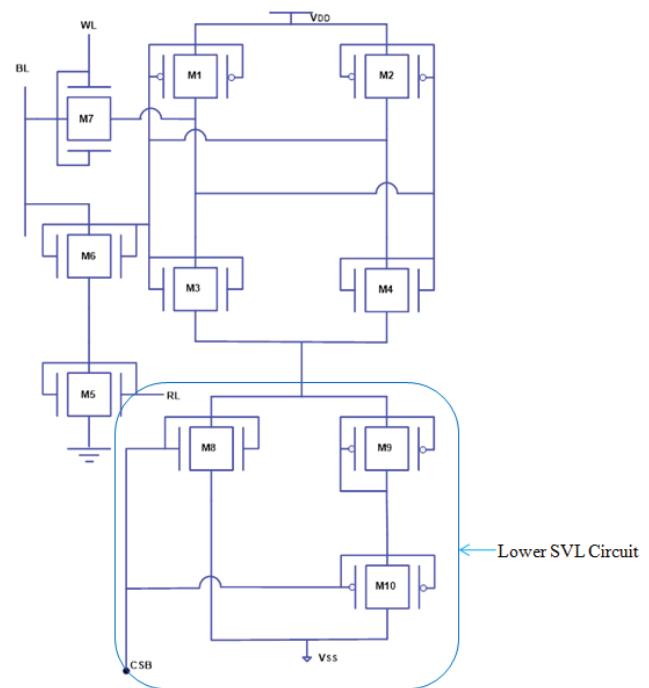


Figure 9. 7T SRAM cell with LSVL approach.

transistors (acting as resistors) arranged in series, joined to a single n-channel type FinFET transistor (functioning as a switch). The USVL circuit is joined with lower side of 7T SRAM cell and CSB signal is used as a controlling signal. In active mode, control signal provides '0' volts, whereas in standby mode, it delivers an increased ground voltage. The LSVL circuit employs the transistor M8 to provide  $V_{ss}$  to the 7T SRAM design. The M9 and M10 transistors are utilized to provide  $V_{ss}$  to the remaining 7T SRAM cell. In the LSVL circuit, the transistors M10 and M8 are activated and deactivated, respectively, when the control signal (CSB) is connected to the power supply ( $V_{ss}=0$  volt). The CSB switch outputs 0 V at ground level when operating in dynamic mode and presents an elevated virtual ground during idle mode. The LSVL approach effectively minimizes leakage flows through transistors M2, M3, and M7. This approach is similar to the diode-footed store structure idea mentioned in [43], which is designed to reduce sub-edge leakages and control signals in a 7T SRAM design that uses FinFET technology. The suggested SRAM utilizing LSVL shows a leakage power of 35.48 nW, which is 31%

higher than hybrid SVL approach and 23.9% higher than the USVL approach.

### 7T SRAM design using hybrid SVL approach

The integration of USVL and LSVL approaches in a 7T SRAM cell utilizing FinFET necessitates the regulating voltage levels within the cell. This regulation is essential for maintaining reliable functionality across diverse operational conditions while also enhancing power efficiency. The integrated strategy is designed to protect the SRAM design against voltage fluctuations that may result in data loss, or potential damage. Implementing proactive control of both upper and lower voltage limits improves reliability, data retention, and longevity. Figure 10 illustrates the circuit of the hybrid SVL approach. In this configuration, the CS and CSB signals function as control signals for the USVL and LSVL circuit respectively.

Figure 10 illustrates the routing of a control signal to the three transistors (M9, M10, and M8) positioned between  $V_{ss}$  and SRAM. The system offers a ground potential and a virtual ground during both active and idle modes, determined by the value of the control signal. Consequently, the leakage current through the M3, M2, and M7 transistors can be minimized. Consequently, reducing gate leakage can lead to a decrease in sub-threshold currents in this context. In the configuration between the 7T SRAM and  $V_{DD}$ , three supplementary transistors are integrated. Transistor P5 is responsible for delivering  $V_{DD}$  to the 7T SRAM during dynamic operation, whereas transistor N8 supplies  $V_{DD}$  when the system is in idle mode. Remaining transistors M1, M4, and M5 minimizes leakage by utilizing the triple transistors located at the upper section. This approach results in a reduction of  $V_{DD}$  to 50% of its original supply, while the ground potential experiences a 25% increase. The hybrid SVL approach increases the  $V_{ss}$  to 0.25 V while decreasing the  $V_{DD}$  to 0.35 V. The hybrid SVL approach demonstrates superior performance compared to individual SVL methods by significantly reducing leakage current and power consumption [44].

## RESULTS AND DISCUSSION

For the suggested SRAM design, the leakage current and leakage power are computed using several leakage reduction approaches, including MTCMOS and SVL. It is discovered that the SVL approach performs better than the MTCMOS approach, which has a 36% reduction in leakage current. The leakage current using the MTCMOS approach is 14.8 nA. All the simulation work done through Cadence Virtuoso Tool. The Total leakage current of the SRAM is given as:

$$I_{\text{leakage}} = I_{\text{Gate}} + I_{\text{sub}} \quad (2)$$

The leakage parameters (power and current) of suggested SRAM design is given in Table 2. The comparative chart of leakage powers and currents for MTCMOS and

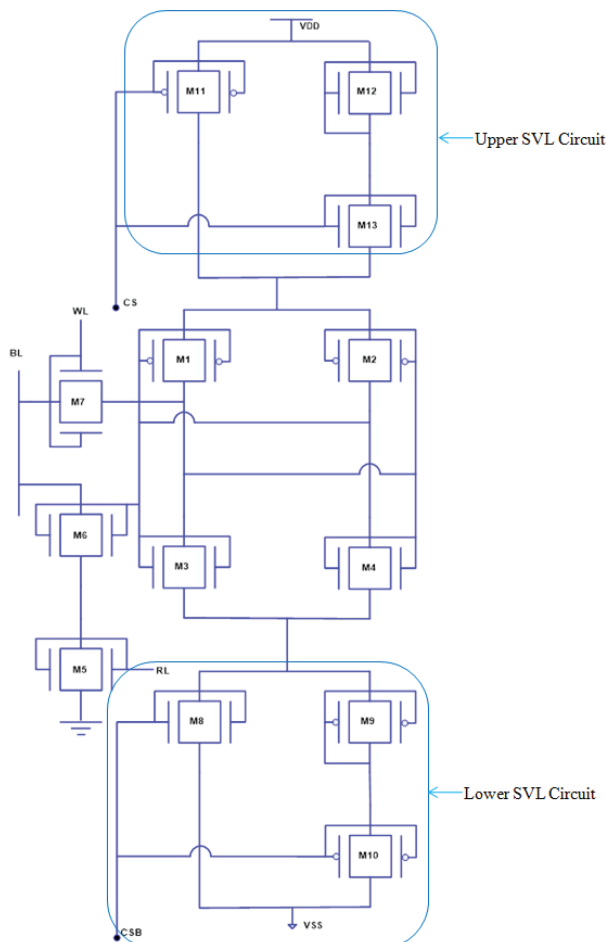
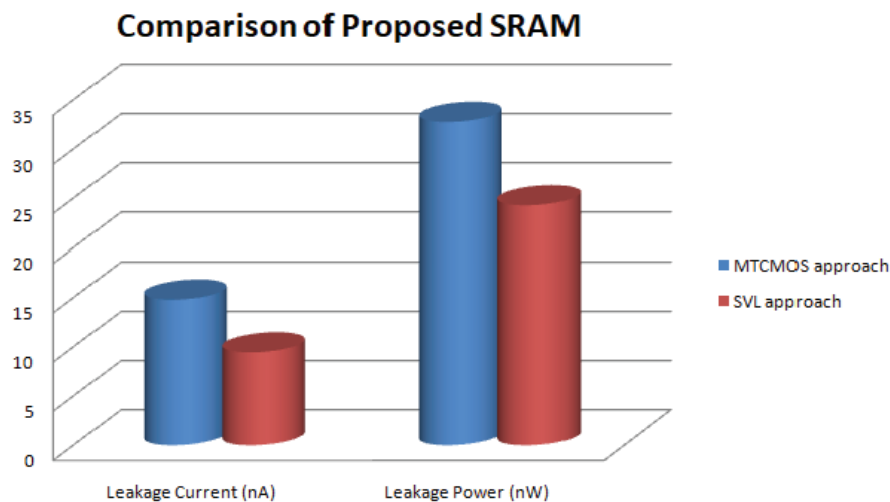


**Figure 10.** 7T SRAM cell hybrid SVL approaches.

**Table 2.** Leakage parameters of Suggested SRAM design

| Suggested Design | Leakage Current (nA) | Leakage Power (nW) |
|------------------|----------------------|--------------------|
| MTCMOS approach  | 14.8                 | 32.76              |
| SVL approach     | 9.45                 | 24.28              |

**Figure 11.** Comparative study of leakage current and power for suggested 7T SRAM design.

SVL approaches is plotted and indicated in Figure 11. The leakage power of suggested SRAM designed with the SVL approach is measured at 24.28nW. This value represents a reduction of 25.8% compared to the power consumption of the SRAM designed with the MTCMOS leakage reduction approach, which is recorded at 32.76 nW.

Since leakage power has emerged as a major performance indicator in nanoscale memory devices, a comparison of the leakage power measured in this work with other relevant works is presented in Table 3 [45-48].

The SRAM's low-leakage design is crucial for implantable devices like cardiac monitors, where long battery life and reliability are essential. The design supports seamless

data collection and transmission in IoT ecosystems, paving the way for advanced remote monitoring solutions.

#### Applications of Suggested SRAM for Internet of Things

Due to the advantages of low power consumption, high speed and scalability, FinFET-based SRAM is widely and effectively applied in IoT. Applications of such are:

1. In wearable devices like fitness trackers and smart-watches, where energy efficiency is important for long battery life.
2. Smart home devices such as smart thermostats, cameras, and voice assistants also use FinFET SRAM, which offers the ability to quickly and efficiently store and access data with minimal power consumption.
3. FinFET SRAM enables real-time processing in edge devices such as sensors and controllers in industrial IoT (IIoT), which are vital for automation, predictive maintenance, and monitoring.
4. Healthcare IoT devices such as portable diagnostics and patient monitoring systems depend on FinFET SRAM for secure and fast data access, low heat dissipation and small form factors.
5. Agricultural IoT is also a beneficiary as smart irrigation and crop monitoring systems need low-power memory for sensors deployed in the field.
6. Fast on-chip memory is required by sensor fusion and decision-making modules used in autonomous vehicles and smart transportation, and FinFET-based SRAM is used for this purpose.

**Table 3.** Comparison of Leakage Power with other relevant works

| Source                              | Leakage Power (nW) |
|-------------------------------------|--------------------|
| Proposed work using SVL approach    | 24.28              |
| Proposed work using MTCMOS approach | 32.76              |
| Standard 7T SRAM [45]               | 35.22              |
| Low Power 7T SRAM [46]              | 36.44              |
| 7T Differential SRAM [47]           | 67.02              |
| Single-Ended 7T SRAM [48]           | 69.1               |

## CONCLUSION

The suggested 7T SRAM using FinFET has been subjected to the leakage reduction approach. It is established that by relating the SVL approach, the leakage current and leakage power are decreased by 36% and 25.8%, respectively, compared to the FinFET-based 7T SRAM with the application of the MTCMOS approach. Implementation of the MTCMOS approach, the leakage current is detected to be 14.8 nA and the leakage power is 32.76 nW. As shown in the results, the analysis of leakage power and leakage current is looked at and contrasted with alternative approaches. The proposed low-power SRAM design leverages FinFET technology to address the unique challenges of healthcare applications. Significant improvements in the power efficiency, stability, and scalability make it ideal for wearable and implantable devices.

Future research may explore advanced transistor technologies such as Gate-All-Around FETs (GAA FETs) and alternative memory technologies like STT-RAM to further enhance the energy efficiency and performance.

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## AUTHORSHIP CONTRIBUTIONS

**Deepak Garg:** Study design, investigation, writing-original draft, editing, methodology and validation.

**Rupali Singh:** Supervision, manuscript review and editing.

## DATA AVAILABILITY STATEMENT

The authors confirm that the data that supports the findings of this study are available within the article. Raw data that support the finding of this study are available from the corresponding author, upon reasonable request.

## CONFLICT OF INTEREST

The author declared no potential conflicts of interest with respect to the research, authorship, and/or publication of this article.

## ETHICS

There are no ethical issues with the publication of this manuscript.

## STATEMENT ON THE USE OF ARTIFICIAL INTELLIGENCE

Artificial intelligence was not used in the preparation of the article.

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