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Research Article

Effect of switching non-linearities on the common mode current in a PV source transformerless inverter in an on-grid system

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ABSTRACT

The integration of solar photovoltaic systems into the grid presents itself with several novel issues that need to be solved before successful integration can be achieved. The problem of common-mode current, also known as leakage current, is one such concern when a transformerless system is preferred due to the benefits it offers. The issue of leakage current has been addressed in the past, but little to no effort has been made towards analyzing the effect of the non-linear behavior of the semiconductor switches used in power converter circuits. This introduces a gap between theoretical and practical results across all past studies. This paper proposes a mathematical analysis of the various non-linearities present in a transistor switch, which is a novel aspect of transformerless inverter circuit analysis and practical feasibility. The mathematical results define the effect of each non-linearity on the harmonic content and, hence, on the leakage current. A simulation-based study was also conducted, comparing the performance of the practical switch and the ideal switch based on common mode current magnitude and other parameters, including total harmonic distortion, ripple content, and root mean square values of the input and output currents and voltages. It was concluded based on simulation results that the leakage current in the presence of such non-linearities is 10 times higher and total harmonic distortion is 3 times higher than that in their absence for a 1kW system, and the rms values of the output voltage and current are also reduced. The findings suggest that the topologies developed for the mitigation of common mode currents must take into account the effect of non-linearities to be feasible for practical deployment.

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INTRODUCTION

The incorporation of renewable energy resources into the grid has gained significant interest in recent times. The solar photovoltaic (SPV) source has promising potential to meet the growing energy demands. However, the integration of SPV source involves several intricacies. The integration issues must be addressed so that the share of renewable energy grows without impediments.

The SPV source is a DC current source that is coupled to the AC load and the grid through an inverter. Naturally, there should be a galvanic isolation between the inverter and the grid. But the transformer installed for this purpose increases losses, volume, and cost, and its elimination results in a system that is more efficient, compact, and economical [1].

The SPV source has parasitic capacitance to ground, which induces common-mode current (CMC). It is necessarily a high-frequency current emanating from the PV source and travelling through the ground back into the system. It poses safety hazards as protective devices based on CMC become futile. Moreover, they introduce harmonics into the grid, and also, the slow deterioration of PV panels has been reported [2,3]. The IEC 62109-2 and VDE-00126 require the CMC to be restricted below 300mA [4,5].

The studies undertaken in this area have sought to explain the factors affecting the CMC phenomenon in grid-connected PV systems and to work out its mathematical formulation. Additionally, this has led to the development of several inverter topologies to mitigate this issue [6,7]. Gubia et al. proposed a model for analyzing the common-mode behavior of a full-bridge inverter circuit powered by a PV source. The model is simplified and

accounts for various conditions of the filter inductor to derive expressions for the CMC and other parameters. It also considers the voltage levels during multiple modes of the output voltage cycle and their effects. While the work claims applicability to various topologies, the generalized procedure has not been proposed [8].

Kerekes et al. analyzed the effects of supply imbalance and neutral conductor on leakage current in prevalent inverter topologies for grid-connected PV systems. The model incorporates various stray and parasitic capacitances and inductances that affect common-mode current flow. It concludes that the neutral line inductance has a considerable effect. The generalized approach is well stated for analysis, but the same has not been employed to derive mathematical expressions for each topology [9].

Chen et al. proposed a pi-circuit model for leakage current based on their method for calculating parasitic capacitance. This model allows consideration of the parasitic components of each PV panel individually, leading to a more realistic analysis than the single-capacitor model. However, the calculation of current based on equivalent resistance lacks a mathematical basis in this study, and verification is based solely on simulation and hardware results [10].

Xiao et al. developed a common-mode analytical model that accounts for all sources of CMC by considering all possible points of parasitic capacitance. The CMV has been related to the equivalent impedance obtained from the developed model. The study, however, lacks consideration of other allied parameters, such as THD and efficiency [11].

Vazquez et al. performed a CMV study for H5, HERIC, and NPC topologies. The focus of the study is switching and conduction losses in the semiconductor switches. The well-known equations have been used for calculation, and the results have been verified through PSIM simulation. The study does not involve an analysis of the eventual effect on the CMC [12].

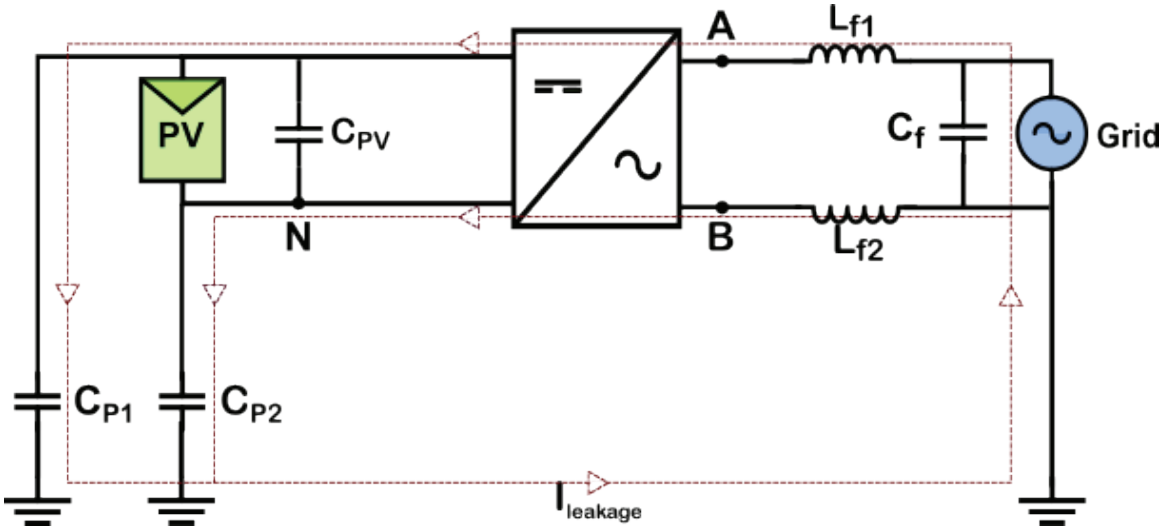

Figure 1. Origin of CMC.

Apart from the mentioned gaps in the study, a prior study on the effect of the non-linearities inherent in semiconductor switches used in power converter circuits has not been reported to the best of the authors' knowledge. The absence of such a study hinders the analysis of the developed inverter topologies in practical scenarios. Furthermore, understanding the effects of non-linearities would motivate the design of novel topologies that are more effective in non-ideal conditions.

This work aims to identify the various types of nonlinearity present in semiconductor switches and to elucidate their effects on the common-mode voltage (CMV) and CMC. Currently, an H-bridge inverter circuit with bipolar modulation is under consideration for analysis. The method can be applied to both unipolar and hybrid modulation. The analytical foundation is first laid for each non-linearity type, which is later validated through simulation.

The rest of the paper is organized as follows. The subsequent section presents the system configuration and its operating principles. Next, the non-linearities and their respective effects have been detailed through analytical treatment. Then, the mathematical results have been validated through simulation. Lastly, the conclusions of the study and the future trends have been stated.

SYSTEM CONFIGURATION & OPERATING PRINCIPLES

The system considered for the study is shown in Figure 1 and 2. It consists of an SPV source coupled to the grid through an inverter. The SPV source has parasitic capacitance to ground, which can be associated with both positive and negative terminals separately, denoted by C_{P1} and C_{P2}, respectively. As the voltage of the positive and the negative terminals jumps with respect to the ground, a current leaks through these capacitances into the ground, which constitutes CMC [13,14]. A large capacitor C_{PV} is installed to reduce the ripples in the input current. The DC output of the PV source is converted to AC of appropriate magnitude and frequency through the inverter for proper coupling with the grid [15].

The inverter circuit is a conventional H-bridge inverter consisting of four bidirectional semiconductor switches. They are switched according to the bipolar modulation technique with a modulation index equal to 1, resulting in two modes of operation. In mode 1, switches S1 and S2 are ON, generating the positive voltage level, whereas in mode 2, switches S3 and S4 are ON, generating the negative voltage level. Therefore, the inverter output would be a two-level output, i.e. $+V_{DC}$ and $-V_{DC}$, which is filtered through an LC low pass filter to obtain the sinusoidal waveform [16,17].

Since the objective of the study is to analyze the effect of the switch's non-linear behavior, several other factors have been assumed constant or ideal. A single-phase system has been used to elucidate the concept, which can, however, be extended to a three-phase system. The solar insolation and the panel temperature are constant [18]. The semiconductor switches are similar in characteristics. The bipolar modulation with a modulation index equal to 1 has been employed, though in practice, unipolar or hybrid modulation with a varying modulation index may be used, requiring extended analysis along the same lines as in this paper. The grid voltage and frequency have been assumed to be constant, which is not the case due to varying loads [19]. The filter is also assumed to be ideal.

For mathematical formulation, let us define the following parameters:

Input Voltage: V_{DC}, Input Current: I_{DC}, Current through a switch: I_{SW}, Gating Voltage: V_G, On-state voltage drop in a semiconductor switch: V_{CES}, Off-state residual current through a semiconductor switch: I_{CES}, Inverter Output Voltage: V_o, Load Voltage: V_L, Load Current: I_L, Load: Z_L, Output Power: P_L, Power Loss: P_{loss}, Modulating signal frequency: ω, Filter Cutoff frequency: ω_f.

The DC voltage level available at the load end is the DC-link voltage minus two times the on-state voltage drops [20]. The expression for the inverter output voltage can be simplified if the input voltage is set to that value. Accordingly, under the ideal and linear case, the inverter output voltage is given as [21]:

$$v_o = \begin{cases} +V_{DC}, & for\ positive\ half\ cycle \\ -V_{DC}, & for\ negative\ half\ cycle \end{cases} \quad (1)$$

It would result in a square wave given by [22]:

$$V_o = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_{DC}}{n\pi} \sin n\omega t \quad (2)$$

If the cut-off frequency is set as: $\omega_f = 5\omega$, the load voltage is given as [23]:

$$V_L = \frac{4V_{DC}}{\pi} \sin \omega t + \frac{4V_{DC}}{3\pi} \sin 2\omega t + \frac{4V_{DC}}{5\pi} \sin 5\omega t \quad (3)$$

Thus, it contains the 3rd and the 5th harmonics with decreasing magnitude. The power loss due to filtered frequency components is given as [24]:

$$P_{loss} = \frac{4{V_{DC}}^2}{\pi^2 Z_L} \left(\frac{1}{49} + \frac{1}{81} + \frac{1}{121} + \cdots \right) \quad (4)$$

The sum converges to 0.083, and the ratio of power loss to useful power is 0.082/1.15 = 0.072 or 7.2 %.

The instantaneous current through a switch can similarly be defined as a piecewise function as follows [21].

$$i_{sw} = \begin{cases} +I_{DC}, & for\ positive\ half\ cycle \\ -I_{DC}, & for\ negative\ half\ cycle \end{cases} \quad (5)$$

The Fourier representation for the ideal and non-linear case is [22]:

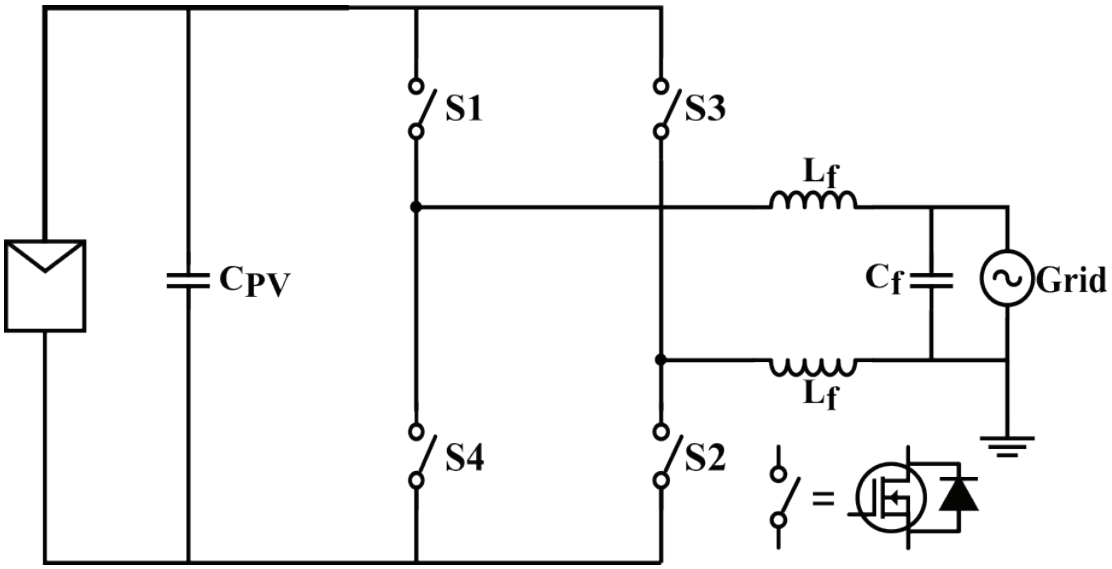

Figure 2. H-bridge inverter.

$$i_{sw} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4I_{DC}}{n\pi} \sin n\omega t \tag{6}$$

Since the common mode current or leakage current is capacitive in nature, its value is given by the equation:

$$I_{CM} = C_P \frac{dV_{CM}}{dt} \tag{7}$$

where I_{CM} is the leakage current, $C_P = C_{P1} + C_{P2}$ is the total parasitic capacitance, and V_{CM} is the common mode voltage given by [25]:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} + (V_{AN} - V_{BN}) \frac{L_{f2} - L_{f1}}{2(L_{f2} + L_{f1})} \tag{8}$$

where V_{AN} & V_{BN} are the voltages of leg A and B of the H-bridge with respect to point N, and L_{f1} & L_{f2} are the filter inductances in the two AC terminals. If they are equal, the equation reduces to [26]:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{9}$$

ANALYTICAL TREATMENT OF THE EFFECTS OF NON-LINEARITIES

The equations 1-4 above pertain to the linear switching behavior. In this section, we present the identified non-linearities and their effect on the output. Let us consider a voltage-switched semiconductor device. The current through the switch is a non-linear function of gate voltage. Hence, the voltage waveform that appears at the inverter terminals as the inverter output V_o, since it depends on switching behavior, will have the reflection of the switching non-linearities [27,28]. Since switching behavior comprises a combination of various non-linearities, we evaluate their effects individually. The typical plots for all the non-linearities are shown in Figure 3(a)-3(d).

Dead Zone

The flow of current is delayed until the gate voltage reaches a threshold value. The dead zone is taken into account by translating into an angle α on the ωt plot having a small value [29]. The dead zone causes departure from the ideal square wave, thus requiring the equations to be reworked. As stated earlier, bipolar modulation has been employed, resulting in two voltage levels. The current through the switch, in contrast with equation 5, is now given as:

$$i_{sw} = \begin{cases} 0, & 0 \le \omega t < \propto \\ I_{sw}, & \alpha \le \omega t < \pi - \alpha \\ 0, & \pi - \alpha \le \omega t < \pi + \alpha \\ -I_{sw}, & \pi + \alpha \le \omega t < 2\pi - \alpha \\ 0, & 2\pi - \alpha \le \omega t < 2\pi \end{cases} \tag{10}$$

The Fourier series for the above waveform is given by [20]:

$$i_{sw} = \sum_{n=1,3,5,\ldots}^{\infty} B_n \sin n\omega t \tag{11}$$

where $B_n = \frac{1}{\pi} \int_0^{2\pi} i_{sw}\, d\omega t$, thus the magnitudes of successive components evaluate to:

$$B_1 = \frac{4I_{sw}}{\pi} \cos\alpha,\ B_3 = \frac{4I_{sw}}{\pi} (-3\cos\alpha + 4cos^3 \propto),$$
$$B_5 = \frac{4I_{sw}}{\pi} (5\cos\alpha - 20\, cos^3 \propto + 16\, cos^5 \propto)$$

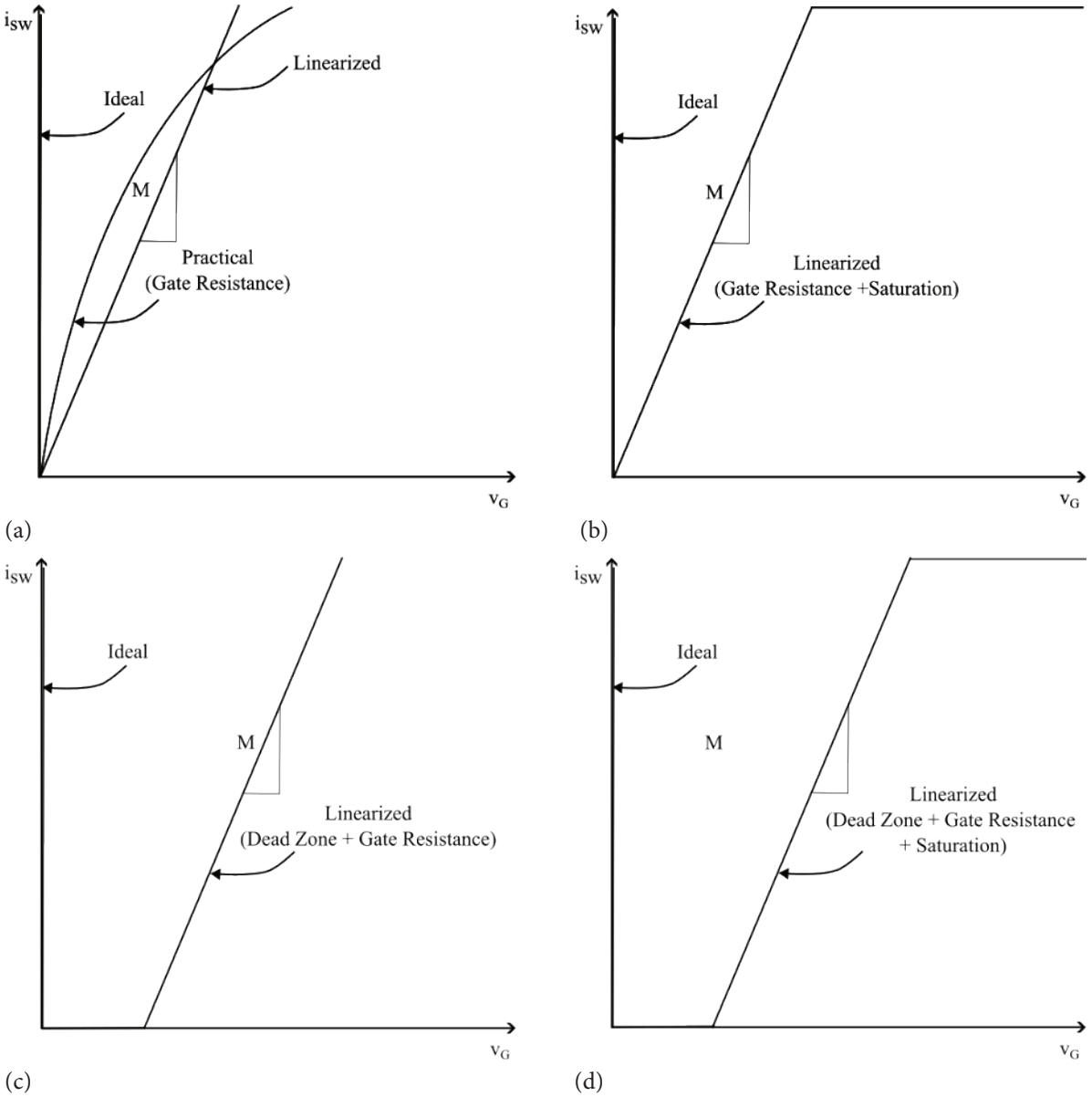

Figure 3. Transfer characteristics of semiconductor switch with: (a) Gate resistance, (b) Gate resistance and saturation, (c) Dead zone and gate resistance, (d) All non-linearities.

The comparison with respective components in equation 3 yields that the magnitude of the fundamental component, as well as the harmonics, is somewhat smaller when the dead zone is introduced. The dead zone non-linearity does not affect the variation of CMV, and hence CMC remains unaffected as well.

Gate Resistance

Ideally, the switch current should be independent of the gate voltage above the latter's threshold value. In a practical switch, there exists a relationship between the two, the ratio of which can be termed gate conductance [30]. To analyze the effect of gate resistance, a linear relationship is assumed from the zero point, i.e., the dead-time non-linearity is ignored. But the gate voltage rises to its final value with a slope (say) M up to (say) β degrees on the ωt plot. The current through the switch, if the gate voltage goes on to rise above the threshold value, is given as:

$$i_{sw} = \begin{cases} M\dfrac{I_{sw}}{V_G}\omega t\,, & 0 \le \omega t < \beta \\ I_{sw}, & \beta \le \omega t < \pi - \beta \\ -M\dfrac{I_{sw}}{V_G}\omega t, & \pi - \beta \le \omega t < \pi + \beta \\ -I_{sw}, & \pi + \beta \le \omega t < 2\pi - \beta \\ M\dfrac{I_{sw}}{V_G}\omega t\,, & 2\pi - \beta \le \omega t < 2\pi \end{cases} \quad (12)$$

The Fourier series coefficients will show a reduction in the magnitudes of all frequency components. Moreover, the piecewise function i_{sw} is indicative of several jumps in voltage of the inverter output terminals A and B. The four discontinuities in each cycle, along with continuous variation in three of the five periods, cause CMV to vary much more severely.

Saturation

If the gate voltage is increased beyond a particular value but within the breakdown point, the switch current becomes constant (=I_{th}) and independent of it. This phenomenon can be termed saturation [31]. In such a case, the current through the switch, while gate resistance is taken into account, is given as:

$$i_{sw} = \begin{cases} M\frac{I_{sw}}{V_G}\omega t\,, & 0 \le \omega t < \beta \\ I_{th}, & \beta \le \omega t < \pi - \beta \\ -M\frac{I_{sw}}{V_G}\omega t, & \pi - \beta \le \omega t < \pi + \beta \\ -I_{th}, & \pi + \beta \le \omega t < 2\pi - \beta \\ M\frac{I_{sw}}{V_G}\omega t\,, & 2\pi - \beta \le \omega t < 2\pi \end{cases} \quad (13)$$

The effect is similar to that in the case of gate resistance, except that the jump is now more severe. This causes still more variation in CMV.

RESULTS AND DISCUSSION

Suspended For a comparison of the common mode behavior under an ideal scenario and a practical scenario where non-linearities are present, a simulation of a PV source H-bridge inverter with bipolar modulation has been performed. The platform for simulation is MATLAB 2024a, but the modelling of the practical switch is done in conjunction with LTSPICE as follows:

(i) Obtain a netlist of the required power electronic device that models the practical switch behavior as per $i_{sw} = f(v_G, v_C)$.
(ii) Interface MATLAB with the LTSpice and sweep through the variables v_G and v_C to generate a 3-dimensional lookup table relating the switch current to the two variables.

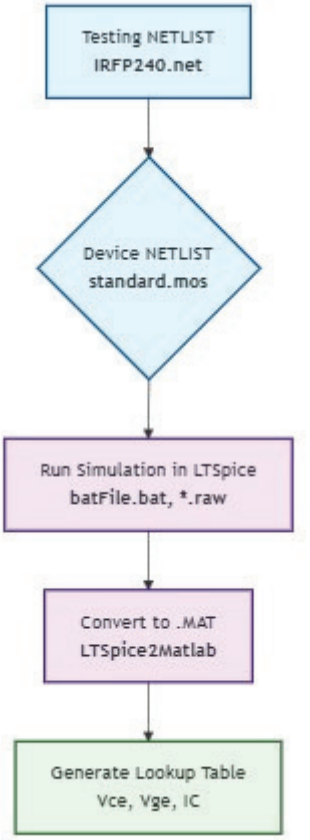

Figure 4. LTSpice and MATLAB interfacing for realizing practical semiconductor switches.

Table 1. Semiconductor switch specification

Parameter	Symbol	Specification
Continuous Drain Current	I_D	20A @ $V_{GS} = 10V$, $T_c = 25°C$
Power Dissipation	P_D	150 W @ $T_c = 25°C$
Gate to Source Voltage	V_{GS}	±20V
Operating and Storage Temperature	T	-50 to +150°C
Drain to Source Breakdown Voltage	$V_{BR(DSS)}$	200V @ $V_{GS} = 0V$, $I_D = 250\mu A$
Drain to Source On-Resistance	$R_{DS(ON)}$	0.18Ω
Gate Threshold Voltage	$V_{GS(th)}$	2-4V @ $V_{DS} = V_{GS}$, $I_D = 250\mu A$
Drain to Source Leakage Current	I_{DSS}	25 -250 μA @ $V_{DS} = 200$ - 160, $V_{GS} = 0V$
Gate to Source Leakage Current	I_{GSS}	-100 to +100 nA @$V_{GS} = 20V$
Turn-on Time	t_{ON}	65 ns @$V_{DD} = 100V$, $I_D = 18A$, $R_G = 9.1\Omega$, $R_D = 5.4\Omega$
Turn-off Time	t_{OFF}	81 ns @ $V_{DD} = 100V$, $I_D = 18A$, $R_G = 9.1\Omega$, $R_D = 5.4\Omega$

(iii) Use the lookup table to generate a base workspace variable in MATLAB to be used in the simulation model to mimic switch behavior.

The workflow has been demonstrated in Figure 4. The suitable environment for simulating the inverter circuit with the practical switch is Simscape, available within the MATLAB platform. It allows the modelling of semiconductor switches through a user-provided lookup table.

The simulation is run for three cycles of grid voltage, i.e., 0.06s for a 50Hz system. The switching behavior is modelled as explained above. The practical switch used in the study is International Rectifier make IRFP240, which is a power MOSFET. The essential switch parameters are listed in Table 1. The following are the simulation parameters:

PV Source: $Tata_{PowerSolar}$: TP330, Solar Insolation = $1000 W/m^2$, C_{PV} = $2200\mu F$, Practical Switch: Make-International Rectifier, IRFP240 HEXFET Power MOSFET, V_{DSS} = $200V$, $R_{DS(on)}$ = 0.18Ω, I_D = $20A$, Filter: L_{f1} = L_{f2} = $30mH$, C_f = $0.1\mu F$, Load = $1kW$, C_P = $2\mu F$, Ground Resistance = 10Ω.

All the performance parameters are listed in Table 2. The transfer and the input-output characteristics are shown

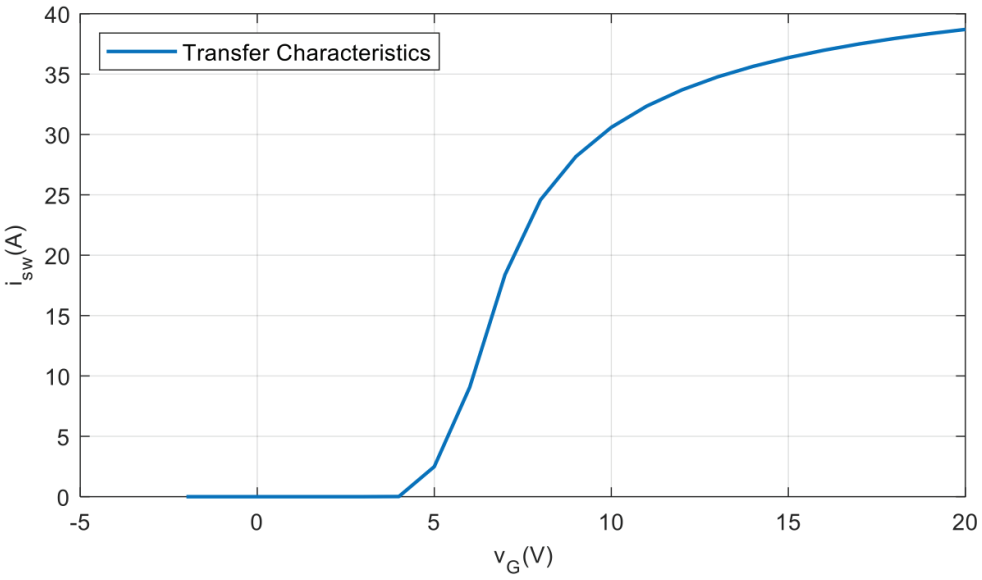

Figure 5. Transfer characteristics of semiconductor switch.

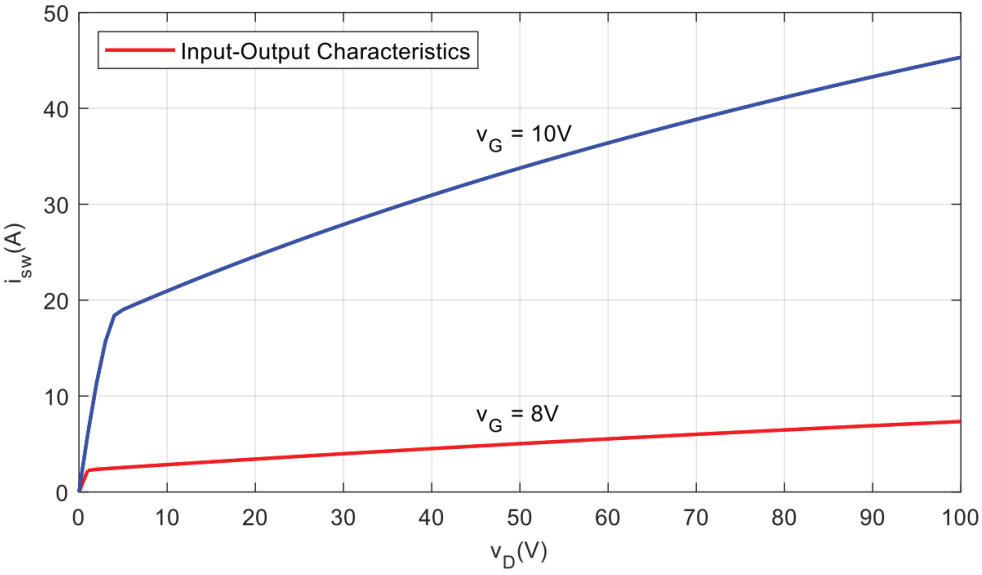

Figure 6. Input characteristics of semiconductor switch.

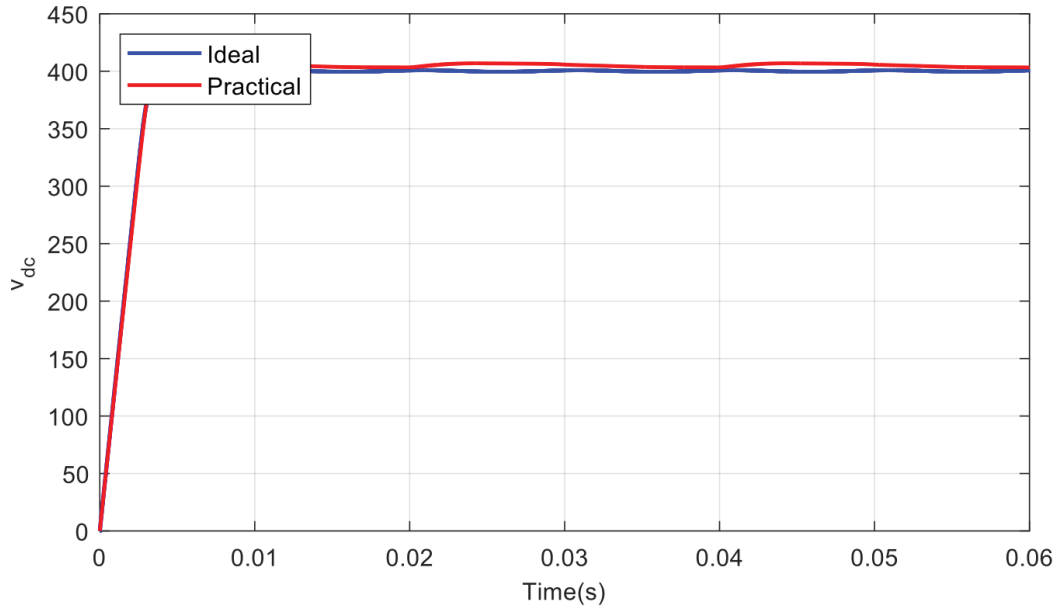

Figure 7. Input DC voltage.

in Figure 5, 6. All sorts of non-linearities discussed above, viz. Dead Zone, Gate Resistance, and Saturation can be observed in the plot. The switch current equals the leakage current below the gate-to-source voltage threshold.

The input voltage waveform is shown in Figure 7. It is the voltage across the DC link capacitor. Even with a heavy DC link capacitor, it still contains ripples that affect the CMV and cause CMCs. The ripple content in the practical case is twice that in the ideal case.

The output voltage and current of the system in both the ideal and practical cases are shown in Figure 8 and 9, respectively. The measurements are taken when no grid is connected to ascertain the output, when the grid does not flatten it.

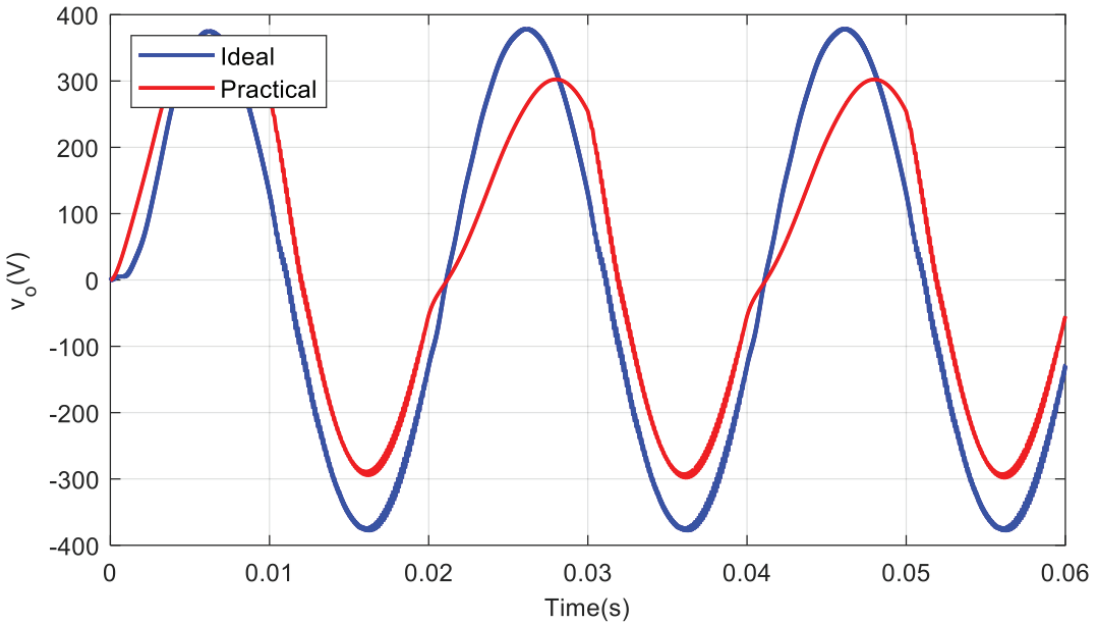

Figure 8. Output AC voltage.

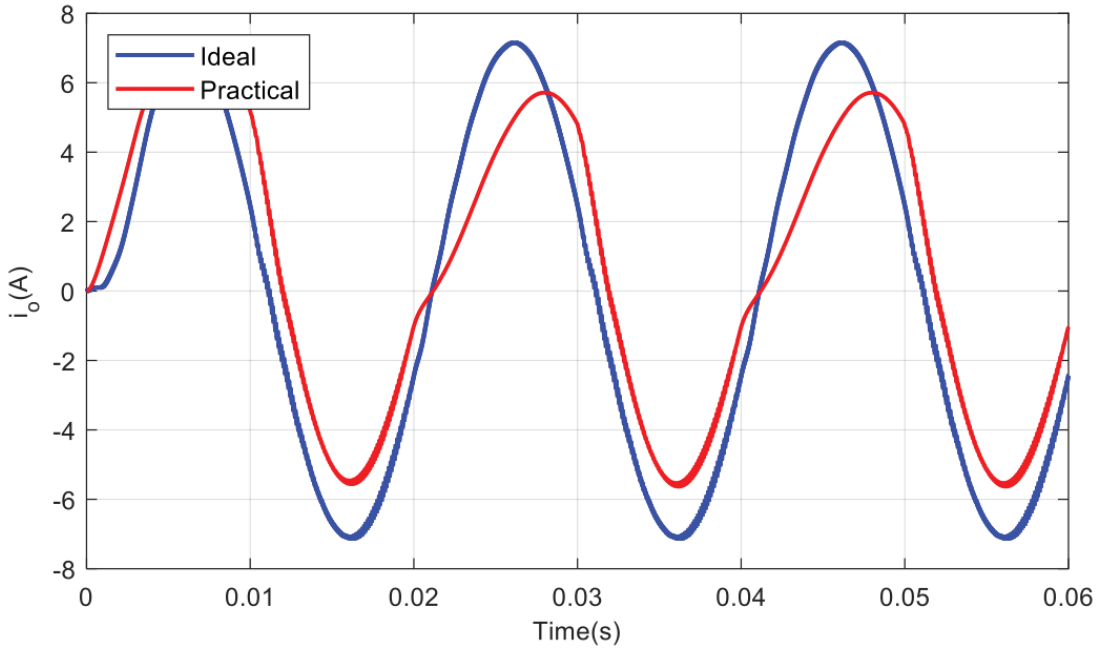

Figure 9. Output AC Current.

Table 2. Comparison between ideal and practical switch-based inverter

Parameter	Ideal switch	Practical switch
Input Voltage (V)	371.42	358.79
Ripple Factor (%)	4.04	11.92
RMS Output Voltage (V)	226.8	202.8
RMS Output Current (A)	4.29	3.93
THD (%)	2.83	8.23
RMS value of CMV (V)	268.32	361.29
RMS value of CMC (mA)	4.2	47.6

A current sensor takes the CMC measurement as it passes through the ground path. In the ideal case, the CMC was observed to be 4.2 mA, compared to 47.6 mA in the practical case for the 1 kW system. On the small scale, an increment of about 10 times was observed. For a larger-scale on-grid PV system, the leakage current will increase proportionally to the scaling and exceed the permissible limit of 300 mA for a 7 kW practical system, as opposed to 70 kW for an ideal switch without targeted mitigation. The waveforms in both cases are shown in Figure 10, 11. Very high-frequency oscillations of large magnitude are observed in the practical case.

The higher CMC will result in the malfunctioning of protective devices. Thus, the safety of life in the vicinity of the system is compromised. Also, the rate of slow deterioration of the PV panel will increase manifold, leading to a decrease in its life. The power loss remains insignificant due to the small magnitude of the CMC, i.e., in the order of milliamperes.

In the ideal case, total harmonic distortion is due to the cut-off frequency being set to 13 times the fundamental frequency. The THD with the practical switch is significantly high, i.e., 8.23%, which can be attributed to non-linear switching behavior. The IEEE 519-2014 standard specifies the THD limit as 8% for bus voltage less than 1 kV [32]. The limit is violated in the practical system, contrary to what is suggested by the simulation results of the ideal system. The higher THD indicates the presence of higher harmonics, causing the CMV to jump even more, and the CMC will be higher. Also, the higher harmonics injected into the grid cause well-known issues, such as crawling in induction motors, inefficient appliance operation, flickering lights, and device overheating.

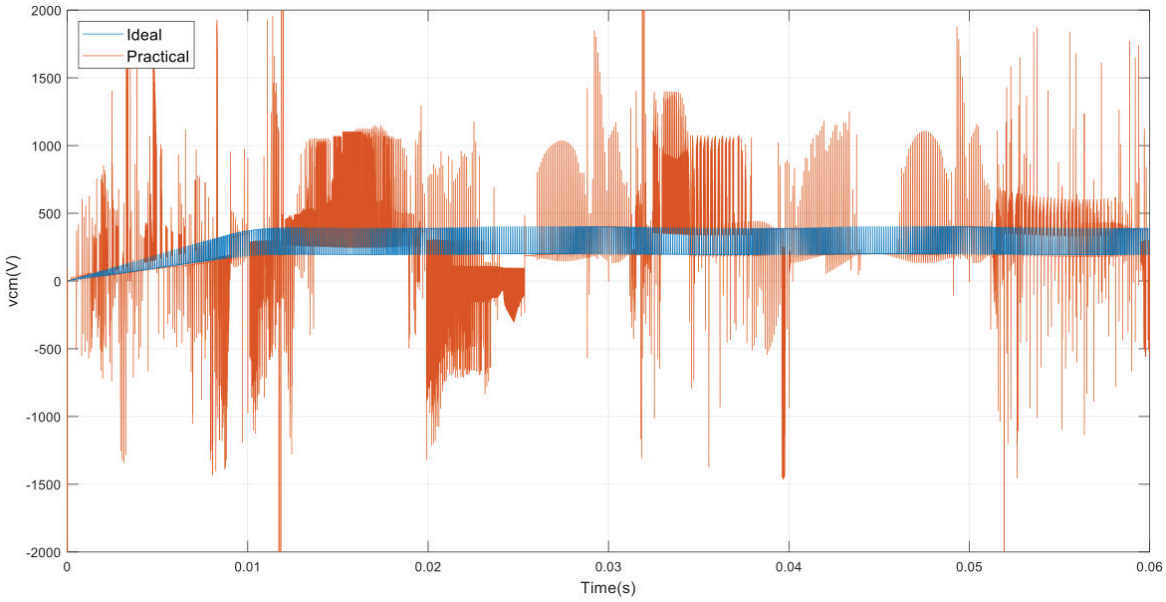

Figure 10. Common mode voltage.

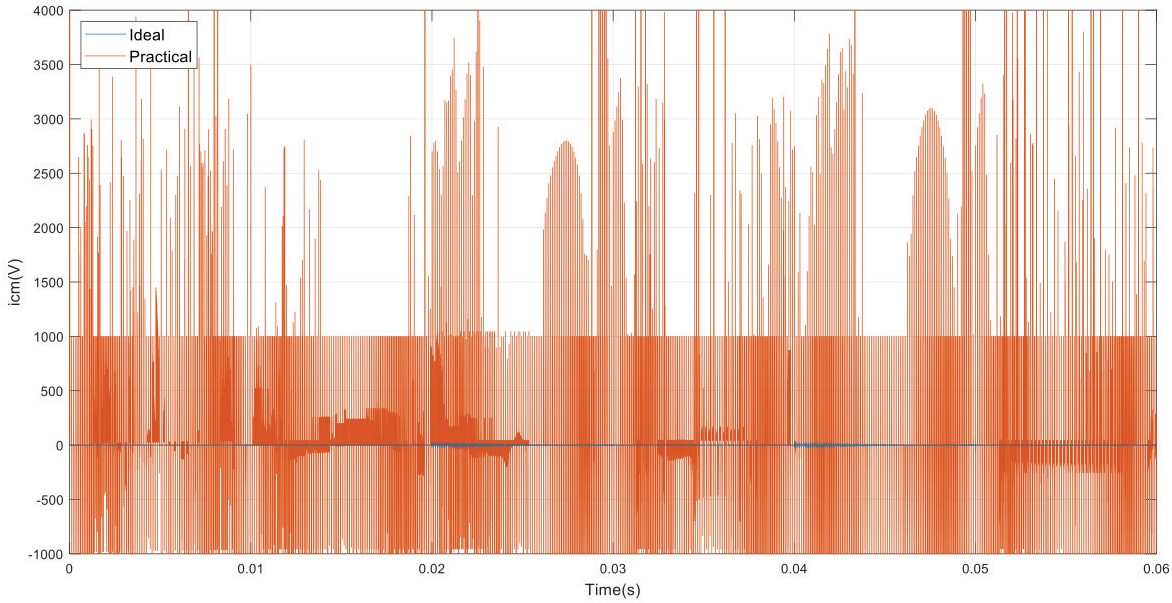

Figure 11. Common mode current.

Owing to the above-discussed issues induced by the non-linear behavior of semiconductor switches, the analysis of transformerless inverters for PV systems should take them into account, and new designs should address the issues they cause.

CONCLUSION

In this study, the non-linearity aspect of the semiconductor switch behavior was considered, and the effect of non-linearities on the common mode current was established both theoretically and practically through simulation. It was concluded that the common mode effect differs significantly in a practical scenario from that predicted by the model simulated with ideal switches. The magnitude of the common mode current was measured at 47.6 mA for practical switches, compared with 4.2 mA for ideal switches, in a 1 kW single-phase application. This multiplies by the size of the system. This framework should help analyze inverter topologies that have been

developed or will be developed in the practical scenario. Also, the total harmonic distortion was found to be 8.23%, compared with 2.83%. This guides the selection of filter parameters in a practical scenario. The fundamental output voltage is also attenuated due to voltage drop and harmonics, implying that more photovoltaic sources in series are required, or a DC-DC converter with higher boosting capability is needed.

This study, as a starting point, was based on bipolar modulation, whereas most, if not all, inverters use unipolar or hybrid modulation. Moreover, the single-phase system was studied. Therefore, future work may focus on establishing the effects of non-linearity in such practical variants of the studied system.

NOMENCLATURE

C_{P1}	Parasitic capacitance of positive PV terminal, F
C_{P2}	Parasitic capacitance of negative PV terminal, F
C_P	Total parasitic capacitance of PV panel, F
C_{PV}	DC link capacitance, F
V_{DC}	Input (DC link) voltage, V
I_{DC}	Input current, A
I_{sw}	Current through switch, A
V_G	Gating Voltage, V
V_{CES}	On-state voltage drop in a switch, V
I_{CES}	Residual current through switch, A
V_o	Inverter output voltage, V
V_L	Load voltage, V
I_L	Load current, A
Z_L	Load impedance, ohm
P_L	Output power, W
P_{loss}	Power loss, W
n	Harmonic
I_{CM}	Common mode current, A
V_{CM}	Common mode voltage, V
V_{AN}	Leg A voltage, V
V_{BN}	Leg B voltage, V
L_f	Filter inductor, H
B_n	Fourier coefficient
M	Slope of gate voltage rise
I_{th}	Switch threshold current, A
v_C	Collector voltage, V
C_f	Filter capacitor, F

Greek symbols

α	Delay angle due to dead zone, °
β	Angle corresponding to the threshold gate voltage, °
ω	Angular frequency, rad/sec

Subscripts

f	Refers to filter
L	Refers to load
P	Refers to parasitic

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