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Research Article

Multilayered full adder layout with wire crossings: A QCA approach to nano computations

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ABSTRACT

Quantum-dot cellular automata (QCA) offer a capable substitute for traditional microelectronics, utilizing quantum mechanics for significantly lower power consumption and enhanced energy efficiency. Adders, essential for arithmetic operations in modern computing, are a key focus within the QCA framework. This work introduces a novel full adder layout featuring a multilayered design with three wire crossings to transfer the binary information in a smooth way without any signal interference. The proposed full adder layout is directly implemented using basic gates and QCA majority voters, not based on a half adder. Compared to previous designs, the proposed layout demonstrates up to a 39% improvement in cell complexity, using three majority gates, thereby being an 83% enhanced design in area-delay cost, proving 56% in area efficiency compared to other relevant designs, indicating the potential for more intricate circuits. The layout was created and simulated using QCADesigner 2.0.3, with total energy estimates reported as 27 *meV* using QCADesigner-E *ver.* 2.2. This analysis is crucial and is avoided in most relevant studies. Notably, this energy-efficient design enhances QCA applicability to more complex circuits by eliminating the need for internal nodes. This advancement in scalability marks a significant step forward in higher-order QCA system design.

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INTRODUCTION

Modern nanotechnologies are being investigated to address the physical limitations of integrated circuits (ICs) fabricated using complementary metal-oxide-semiconductor (CMOS) technology. CMOS-based ICs face challenges such as the high costs associated with lithography, short channel effects, and doping fluctuations, all of which complicate the continued adherence to Moore's law for integrated devices. Quantum-dot Cellular Automata (QCA) represents a notable and burgeoning approach that has garnered significant interest [1]. This cutting-edge technology, operating at high speed, allows for the creation of digital circuits that offer notable benefits, including extremely small power consumption and high packaging density.

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However, QCA technology has to overcome several challenges to become practical and feasible for large-scale digital circuit construction [2].

In QCA, binary or logic information is presented by the positions of electrons within quantum dots. These quantum dots in a cell are arranged in a regular grid, with neighboring dots interacting electrostatically within a finite state machine framework known as an automaton (plural: automata). When electrons are placed within the quantum dots, their electrostatic interactions affect the positioning of adjacent electrons. These electrons experience Coulomb repulsion (like charges repel) and attraction (opposite charges attract) from neighboring electrons, resulting in the collective behavior of electron charges within the cellular automaton [3].

QCA technology introduces a novel perspective on circuit design, offering an innovative method for designing reliability-verified circuits using simulation or prototyping in nanoscale computing [4]. Full adders, fundamental to addition, multiplication, subtraction, and division—the core arithmetic operations in computing—are vital components. High-performance arithmetic circuits hinge on the efficiency of adders. This work introduces a new QCA full adder design that demonstrates substantial improvements over previous designs.

There are two primary approaches to designing QCA circuits: multilayer and coplanar. Multilayer crossovers represent a major advancement in interconnection technology, offering significant advantages over coplanar crossovers. They effectively reduce crosstalk between adjacent signal lines by stacking signal paths vertically in different layers, which isolates signals and enhances signal integrity and reliability, which is crucial in densely packed integrated circuits [5].

This paper proposes a multilayered full adder circuit that enhances performance using a novel algorithm and three-input majority voters in a simplified design. Employing a cell interaction approach reduces the complexity associated with majority gates, inverters, and wire crossings. Unlike designs that use a half adder, this full adder layout directly implements basic gates and QCA majority voters. By optimizing with an appropriate clocking scheme, the design offers improved performance despite the increased layers and cost associated with additional QCA logical devices.

Literature Review

A survey of current full adders was constructed with QCA technology, examining both single-layer and multilayer layouts incorporating QCA crossovers. It outlines the design characteristics, suitability, and limitations of these implementations. The majority of existing designs adopt single-layer configurations with coplanar crossovers, although a minority employ crossovers in different quantities based on the authors' design choices.

In [6], the authors introduced a full adder architecture with many layers where all input and output cells are located in the bottom layer. This configuration utilizes a total of 80 QCA cells spread across three layers, achieving a delay of 0.75-clock cycle. Moreover, the lower layer incorporates two 3-input majority gates and one inverter. M. Amiri *et al.* in [7] proposed an area-efficient single-layer coplanar full adder design, where 62 cells are arranged in such a way within 0.05 μm^2 of an area with a latency of one clock cycle. This design utilizes three majority gates with an inverter, and there are two required wire crossings. When utilizing coplanar crossovers, there is a chance of signal interference, which sometimes makes the circuit vulnerable. A recent study in [8] introduced a single-layer full adder/subtractor design with a one-clock-cycle latency, using 96 cells in a 0.04 μm^2 area. This design includes four majority gates and one inverter, along with two coplanar crossovers, which could be adapted for more complex circuits. Another study proposed a one-bit testable three-layer full adder [9] with 128 quantum-dot cells, also operating at a one-clock-cycle latency. This design uses six majority gates in the first layer and requires four multilayer crossovers. A different single-layer full adder was presented in [10] with 389 QCA cells and a 4.75-clock-cycle delay, employing three majority gates, two inverters, and coplanar crossover by adjusting cell clocking schemes. This design was later expanded for use in advanced circuits like multiply-accumulate units (MAC).

Further research demonstrated a coplanar full adder with three majority gates and six inverters, using 114 cells [11] and a 1.25-clock-cycle latency. Here, crossover was achieved by modifying the clocking scheme of the crossing wires. In [12], Zhang et al. presented five single-layer full adders with scalable designs based on three-input and five-input majority gates, eliminating the need for crossovers. These designs vary in cell count and latency. A separate single-layer full adder with 90 cells, five majority gates, and two inverters was also proposed in [13], avoiding crossovers but incorporating input nodes that restrict further development. However, this design has a higher cost compared to other single-layer adders.

Despite these advancements, several limitations remain. Many designs rely on coplanar crossovers, which can cause signal interference and crosstalk, reducing circuit performance and increasing design complexity. Additionally, energy efficiency, a major advantage of QCA nanotechnology, is often overlooked in these studies. Without proper energy analysis, it's difficult to assess power consumption or compare different designs effectively. This gap makes it challenging to fully evaluate QCA's potential for low-power applications.

The suggested multilayered full-adder design addresses these gaps effectively. By avoiding coplanar crossovers and instead using multilayer crossovers, we reduce the risk of signal interference and crosstalk, leading to a more reliable and scalable design. Additionally, our energy-efficient

design is well-optimized to minimize latency as much as possible, ensuring high-speed operation that meets the demands of advanced nanocomputing.

Key Contributions

The proposed work offers the following key contributions:

(i) The optimized circuit architecture demonstrates significantly reduced energy dissipation while maintaining high-speed operation, making it suitable for low-power nanocomputing applications.

(ii) By employing multilayer crossovers instead of traditional coplanar approaches, the design eliminates internal node dependencies, thereby reducing structural complexity, lowering power consumption, and enhancing scalability for large-scale QCA implementations.

(iii) The design achieves an optimal balance between low latency, high operational speed, minimal energy requirements, and compact area utilization, making it as an efficient solution for advanced QCA systems.

Organization

The structure of the next parts of this article are as follows: Section 2 (Theory) explains the fundamental terminologies to familiarize readers with QCA technology, followed by the proposed circuit's theoretical background. Section 3 (Proposed Work) describes the proposed work as well as design layouts and design parameters, while Section 4 (Results and Discussion) analyzes the corresponding outputs of the suggested design and assesses QCA cost and energy dissipation. Section 5 (Comparisons) compares significant findings with prior relevant studies. Finally, Section 6 sums up the article.

Theory

This section consists of some basic elements of QCA circuitry, which are often needed to create a logic circuit, as well as the theoretical background of a full adder circuit based on an algorithm in the field of digital electronics.

Technological Background

All QCA designs employ some of the most fundamental terms associated with this technology. Here is an explanation of them:

A quantum dot cell or QCA cell comprises four quantum dots positioned at the corners of a square, forming the basic unit cell of QCA. Each QCA cell measures 18 *nm* in length, with a total area of 324 nm^2. The quantum dots are typically nanoscale in size, with diameters of 5 *nm*. Binary logic-1 and logic-0 polarization states, determined by electron locations [3], are shown in Figure 1(a). Two electrons are involved in tunnelling between dots, and because of Coulomb repulsion, the ground state electrons must occupy opposite corners of the square. This results in polarizations of p = +1 and p = -1, representing bit values of 1 and 0, respectively. When both electrons are at the cell's center, it is termed null, indicating the absence of stored data [3].

The QCA inverter (QI), a fundamental logic component in QCA technology, is illustrated in Figure 1(b). This structure inverts the input signal—when the input cell is at logic '0', the output becomes logic '1', and vice versa [3]. Figure 1(c) presents a conventional QCA wire layout, formed by an array of QCA cells. These wires are categorized into two types: standard binary wires and inverter-based chains [3].

A key element in QCA circuit design is the majority voter (MV) or majority gate (MG), composed of five QCA cells—three inputs, one output, and a central cell that determines the result. The gate operates based on majority logic, where the output reflects the dominant state among the three inputs (A, B, and C). Its functionality is mathematically expressed as M(A, B, C), processing the three input signals to produce the corresponding output.

$$M(A,B,C) = AB + BC + CA \tag{1}$$

In QCA technology, basic logic gates such as AND and OR can be constructed by fixing one input of a majority gate to a constant value. For example, setting input C to logic '1' converts the majority gate into a two-input OR gate, while setting C to '0' transforms it into a two-input AND gate [3]. The placement of QCA cells on the substrate is managed by an algorithmic process, with signal propagation controlled through a four-phase clocking scheme. This clocking system not only synchronizes data flow but also provides the energy required for computations.

Unlike traditional approaches that clock cells individually, QCA architecture groups cells into clock zones that operate simultaneously. The QCA clock cycles through four distinct phases—switch, hold, release, and relax—each separated by a 90-degree phase shift. During the switch phase, the tunneling barrier between quantum dots begins to increase. In the hold phase, the barrier remains high, locking the cell's state. The release phase lowers the barrier, and finally, in the relax phase, the cell becomes unpolarized with no inter-dot barrier [5]. This mechanism ensures controlled and efficient data transfer across the QCA circuit.

By adjusting these barriers through clocking, the barriers can be lowered to allow electrons to move, enabling the cell to switch states based on the influence of neighboring cells. When the barriers are raised, the electrons are locked in place, stabilizing the cell's state and allowing information to be transferred smoothly through the QCA circuit. This clocking process ensures that information flows efficiently and with minimal energy use, enabling the precise operation of complex logic functions in QCA-based systems.

Theoretical Background of the Proposed Work

A full adder is an important electronic circuit in computing that takes three input bits and generates two output bits: a sum and a carry-out. With input operands A, B, and C_{in} representing the carry-in, the circuit performs an XOR operation on these three inputs to produce the

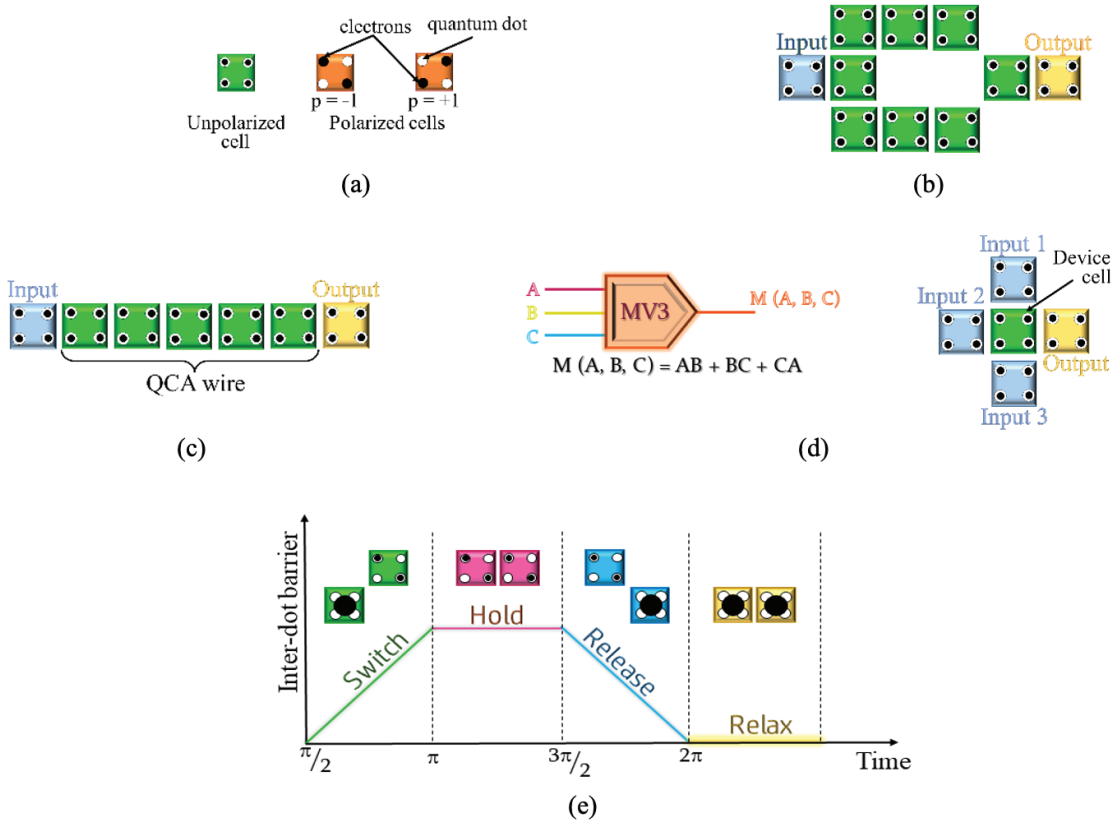


Figure 1. QCA cells and basic devices. (a) QCA cells, (b) QI, (c) wire, (d) majority voting gate (MV3) and (e) clock-zone specific phases

sum output. Additionally, the circuit generates a carry-out (C_{OUT}) through AND and OR operations. The truth table for the full adder circuit's input-output behavior is presented in Table I. The full adder's logical operation, which processes three inputs (A, B, and C_{in}), can be expressed through the following Boolean functions:

$$SUM = A \oplus B \oplus C_{in} \quad (2)$$

$$C_{OUT} = A.B + C_{in}.(A + B) \quad (3)$$

Based on these, it has been proved in [14] that,

$$C_{OUT} = Maj\ (A, B, C_{in}) \quad (4)$$

$$SUM = Maj\ (C_{OUT}, C_{in}, Maj\ (A, B, C_{in})) \quad (5)$$

Drawing inspiration from [14], this work is tailored for three inputs, imposing limitations on implementing a full adder solely based on a half adder. However, the proposed full adder layout circumvents this constraint by directly employing basic gates and QCA majority voters, eliminating the need for a half adder. The connection diagram of the proposed design is illustrated in Figure 2.

Table 1. Logic table of a full adder

Inputs			Outputs*	
A	B	C_{in}	SUM	COUT
0	0	0	L	L
0	0	1	H	L
0	1	0	H	L
0	1	1	L	H
1	0	0	H	L
1	0	1	L	H
1	1	0	L	H
1	1	1	H	H

*L=0, H=1

PROPOSED WORK

This section describes the design of a proposed full adder circuit implemented using QCA technology. However, designing an area-efficient full adder within the QCA framework presents unique challenges, particularly in managing signal routing and minimizing energy dissipation to make the circuit more energy efficient than that

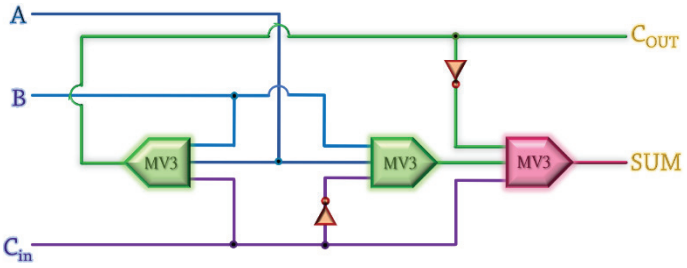


Figure 2. Schematic of the proposed design.

in microelectronics while lowering the latency in output as much as possible to achieve a high operational speed. Addressing these challenges requires innovative design strategies that optimize both the layout and the overall architecture of the circuit.

Methodology

In QCA circuit design, a grid-based cell placement of an array of cells is meticulously drawn according to the schematic produced by a particular logic circuit to form QCA wires and logic gates, enabling the transfer of binary information from input to output nodes. Proper clocking is applied to each cell to ensure synchronized data flow throughout the circuit. Once the clocking is set up under a specific mechanism, the circuit is simulated immediately to check if it produces the correct output. If the output does not match the expected logic table, the clocking can be modified, and the simulation can be rerun. This iterative process continues until the circuit produces the correct output without errors, ensuring the design's accuracy and reliability, as illustrated in Figure 3. Moreover, the cell count in each QCA wire is determined on a trial-and-error basis by simulating the circuit again and again till the correct output reaches a better polarization level.

Positioning the input and output nodes externally to the main architecture enhances scalability and reliability. Multilayer crossover implementation is a good practice to facilitate smooth signal transmission, especially in complex circuits, allowing signals to intersect without interference. This approach reduces circuit complexity and contributes to high-speed operation while maintaining ultra-low power consumption.

Design Layout

During the design phase of a circuit, a well-known simulation tool in this field named QCADesigner [15] *ver.*

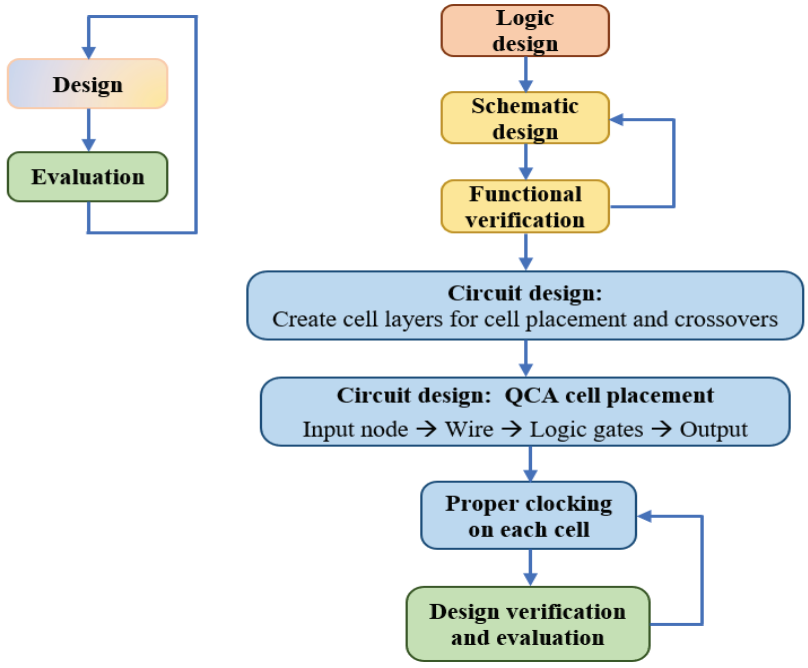
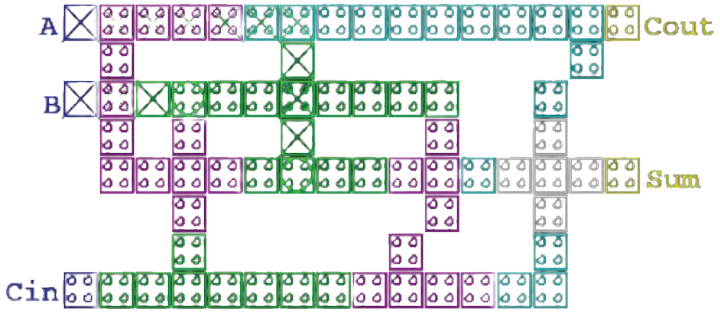


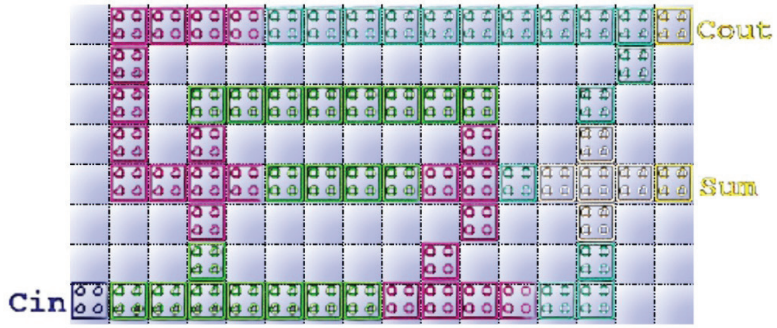
Figure 3. Circuit design flow in QCA during design phase.

2.0.3 is also utilized to simulate and observe the result of the output. The proposed three-input full adder employs a three-layer QCA structure with 83 cells, achieving a latency of just one clock cycle. As shown in Figure 4(a), the design incorporates three MV3 and two QI. Each square QCA cell measures 324 nm^2 with a 2 nm separation between them, resulting in a compact total area of 0.06 μm^2, meaning cells occupy only 45% of the layout space.

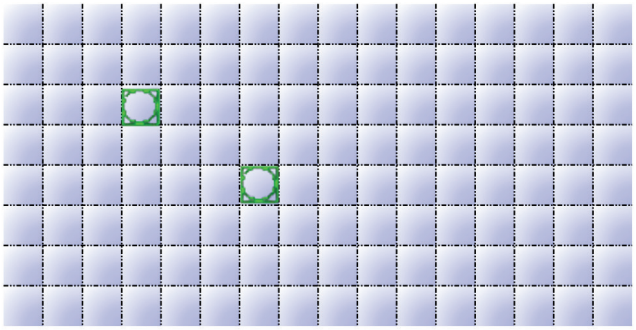
To ensure efficient signal routing, the design uses three multilayer wire crossovers. Input and output nodes



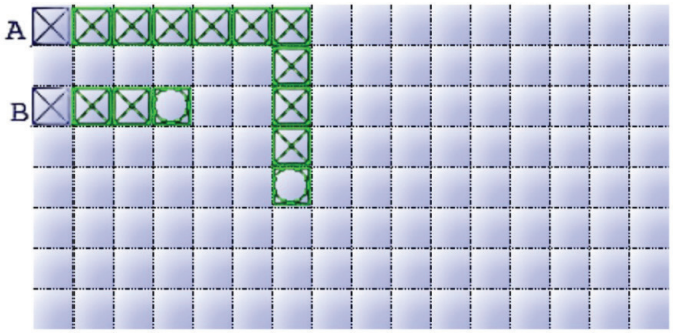
(a)



(b)



(c)



(d)

Figure 4. Proposed design. (a) QCA layout, (b) layer-1 grid layout, (c) layer-2 grid layout, and (d) layer-3 grid layout.

are strategically placed: one input and one output node reside on the primary layer (layer-1), while the remaining input-output nodes are positioned on the top layer (layer-3). A middle layer (layer-2) facilitates interlayer connectivity. The layer-by-layer cell distribution is illustrated in Figure 4(b)–(d). Notably, the architecture avoids fixed-polarized or rotated cells between input and output nodes, maintaining signal integrity and simplifying fabrication.

RESULTS AND DISCUSSION

The proposed design is created using QCA Designer [15] *ver.* 2.0.3, a renowned simulation tool tailored for evaluating QCA circuit performance. Within this tool, the Bistable Approximation Engine is hereby utilized to determine the state of a QCA cell via a time-dependent approach. The cell-level methodology (one cell influencing another) is used to obtain the output. The simulation results verify the output values against the truth table, as depicted in Figure 5. A one-clock delay is also presented in the figure, and after that delay, the outputs are shown as per the input bits received in the circuit. It is highlighted in the red block, and arrows show the first outputs based on the first input bits. It is evident from the QCA layouts presented that the proposed design is accurate and operates according to logic Table 1 without any technical error.

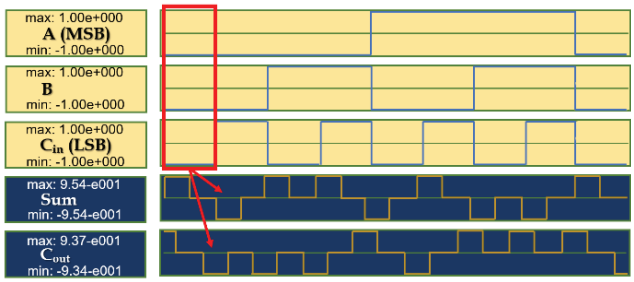


Figure 5. Simulation output of the proposed circuit design.

It is also evident from the simulation that the outputs reach polarizations of more than 0.9, and hence, the efficiency of this nanocircuit is evaluated from the polarization values shown in the above figure.

This work evaluated the energy dissipation of the proposed design using the QCADesigner-E, i.e., QD-E tool [16] *ver.* 2.2. Being an extension of QCADesigner [15] application software, it is used to evaluate the energy dissipation of a multilayered QCA circuit. The total energy dissipation reported using this tool is 27 *meV*, with an average energy dissipation per cycle of 2.45 *meV*. Additionally, this experiment conducted an extensive cost analysis of the proposed QCA circuit, which includes three different types of cost functions [17–18], outlined below.

$$Area\text{-}delay\ cost\ (ADC) = total\ area \times delay^2 \quad (6)$$

$$Energy\text{-}delay\ cost\ (EDC) = energy^2 \times delay^2 \quad (7)$$

$$QCA\text{-}specific\ cost\ (QSC) = n[MV^2 + QI^2 + wC^2] \times delay^2 \quad (8)$$

Here, MV, NG, and WC denote the number of majority gates, not gates, and wire crossings in the proposed design, respectively, while *n* indicates the number of layers. According to equations (6)–(8), the ADC, ESC, and QSC of the suggested circuit are 0.06 units, 0.00073 units, and 66 units, respectively.

In essence, this design lies in a well-organized layout utilizing multilayer crossovers. Typically, QCA designs rely on internal nodes to manage data flow, but these nodes can

Table 2. Comparison of previous and proposed circuit design parameters

Works	Year	Cell count	Total area in μm²	Delay in clock-cycles	Layer type	Crossover type
[6]	2024	80	0.06	0.75	Multiple	ML
[7]	2024	62	0.05	1.00	Single	CP
[8]	2023	96	0.08	1.00	Single	CP
[9]	2020	128	0.15	1.00	Multiple	ML
[10]	2019	389	0.78	4.75	Single	CP
[11]	2019	114	0.23	1.25	Single	CP
[12]	2018	132	0.12	0.75	Single	NA
[12]	2018	115	0.11	0.75	Single	NA
[12]	2018	155	0.15	1.00	Single	NA
[12]	2018	140	0.14	1.00	Single	NA
[12]	2018	118	0.10	0.75	Single	NA
[13]	2016	90	0.07	2.00	Single	NA
Proposed	NA	83	0.06	1.00	Multiple	ML

CP: QCA coplanar crossover; ML: QCA multilayer crossover; NA: Not applicable.

Table 3. Comparison of energy dissipations and cost function estimations

Works	#M	#QI	#wC	TE (*meV*)	Cost functions		
					ADC	EDC	QSC
[6]	2	1	4	NA	0.015	NA	15.8
[7]	3	1	2	NA	0.05	NA	14
[8]	4	1	2	NA	0.08	NA	21
[9]	6	0	4	NA	0.15	NA	156
[10]	3	2	4	NA	17.6	NA	654.3
[11]	3	6	2	NA	0.359	NA	76.6
[12]	3	2	0	283[a]	0.067	0.159	7.31
[12]	3	0	0	249[a]	0.062	0.14	5.06
[12]	3	2	0	327[a]	0.15	0.327	13
[12]	3	0	0	306[a]	0.14	0.306	9
[12]	2	2	0	246[a]	0.056	0.138	4.50
[13]	5	2	0	NA	0.28	NA	116
Proposed	3	2	3	27[b]	0.06	0.0007	66

#: count; TE: Total energy evaluated in *meV*; NA: Not applicable.

[a] Energy assessed at 0.5 E_K using the QCAPro tool

[b] Energy assessed using the QD-E tool

add complexity and reduce efficiency by increasing power consumption and slowing down operations. By avoiding internal nodes, this new design overcomes these issues, resulting in a more streamlined and optimized circuit. The use of multilayer crossovers is particularly innovative because it allows for efficient signal routing without the drawbacks of internal nodes. This makes the design more efficient and easier to scale up for use in more complex QCA circuits.

Moreover, the latency and total energy values of this QCA circuit are critical in determining its overall efficiency. This design becomes area-efficient and energy-efficient by dissipating minimal energy and operating at high speed while occupying a very small area, making it an excellent choice in the context of advanced nanocomputing applications.

Comparisons

Several comparison parameters have been outlined in Table 2 to evaluate the proposed design. This table summarizes the design aspects of the full adder alongside previously reported similar designs. Key comparison metrics include cell complexity, total occupied area, latency, and the type of QCA crossover used.

For example, compared to the latest best full adder design described in [8], the proposed design demonstrates a 14% improvement in cell count and, thereby, a 56% enhancement in total area usage. Additionally, the suggested design effectively utilizes multilayered crossovers to prevent signal interference, a significant improvement over the design in [8], which employs coplanar crossovers and fails to isolate interwire signals.

The comparison with established designs reveals that the proposed full adder exhibits significant performance across various parameters and costs, suggesting its suitability for higher-order designs. Table III provides a comprehensive breakdown of this comparison. Considering another scalable coplanar full adder design [11] based on the same algorithm, the suggested design has likewise managed to achieve an 83% superiority in terms of area-delay cost and, thereby, a 14% enhancement in QCA-specific cost and obviously, this approach successfully uses multilayered crossovers to avoid the signal interference.

In addition, those two papers and a few other recent innovative works did not analyze any energy dissipation of their suggested circuits. However, this work was done in the tables below, including energy dissipation, three costs, and several design parameters. The suggested full adder achieves an energy dissipation of 27 *meV*, a factor overlooked in most existing designs, as tabulated above.

CONCLUSION

The study and implementation of the proposed QCA-based one-bit full adder mark a significant advancement in nanoelectronics, highlighting the importance of efficient design practices. These practices include optimizing cell placement, reducing area usage, and minimizing latency. The proposed design is based on a unique modular algorithm, which shows a modest yet promising progression in creating innovative QCA circuits. This design features

multilayered crossovers with full input-output accessibility. This approach helps avoid crosstalk and supports the development of higher-order circuits. Additionally, this study provides a comprehensive evaluation of energy dissipation and cost functions, offering valuable insights into the performance characteristics of the proposed energy-efficient design. The proposed full adder layout does not utilize a half adder. Rather, it directly implements a full adder employing basic gates and QCA majority voters. This design is not reliant on a half-adder. This scalable design is highly suitable for applications in nanocomputing, such as high-speed arithmetic operations in nano-processors, energy-efficient computing for portable and wearable devices, scalable nanoprocessor architectures, quantum computing systems, advanced signal processing, nanocommunication systems, and neuromorphic computing, where its combination of low latency, minimal energy dissipation, and scalability provides significant advantages.

We plan to fabricate this circuit in the future and extend this work by connecting multiple one-bit full adders to create an n-bit ripple carry adder. We aim to maintain the same clocking scheme and latency, ensuring a consistent and efficient design.

AUTHORSHIP CONTRIBUTIONS

Authors equally contributed to this work.

DATA AVAILABILITY STATEMENT

The authors confirm that the data that supports the findings of this study are available within the article. Raw data that support the findings of this study are available from the corresponding author upon reasonable request.

CONFLICT OF INTEREST

The author declared no potential conflicts of interest with respect to the research, authorship, and/or publication of this article.

ETHICS

There are no ethical issues with the publication of this manuscript.

STATEMENT ON THE USE OF ARTIFICIAL INTELLIGENCE

Artificial intelligence was not used in the preparation of the article.

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