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Research Article

Geometric modification and placement of high heat flux ic chips on substrates of different materials for enhanced heat transfer

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ABSTRACT

This article presents the significance of using different sizes and positions of IC (Integrated Circuit) chips that are mounted on substrates of different materials. 1631The ICs are cooled by forced convection in a horizontal wind tunnel. COMSOL Multiphysics 5.4 solve the IC chip cooling problem by selecting a conjugate heat transfer module with laminar flow. FR4, ba-kelite, single and multi-layer copper clad boards are used as substrate materials. Numerical simulations are performed for FR4, bakelite with a constant heat flux of 5000 W/m^{2,} at 2.5 m/s air velocity. In contrast, single and multi-layer copper clad boards are studied for 10000 W/m^2 with 1.5 m/s air velocity. The prime objective of this research is to use adequate size and placement of chips generating high heat fluxes for enhanced heat transfer. Results showed that larger chips placed at bottom rows and sequentially decreasing sizes in the subsequent rows for the same overall input for high substrate thermal conductivity give more heat dissipation. Among all configurations A0 – F considered in the study, case E provides minimum tempera-ture using single and multi-layer copper clad boards. In addition to modification of chip sizes, geometric spacing of X1/X2 = 1.8 results in lower maximum temperature.

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INTRODUCTION

In recent years, circuit miniaturization in the field of electronics has culminated in the need for effective heat dissipation due to high heat flux densities. Forced convection cooling methods are used as the solution to this challenge. Moreover, geometric modifications and the optimal arrangement of IC chips result in effective heat dissipation. This work mainly applies to small electronic equipment, viz., personal computers, laptops, digital cameras, etc. These devices use a substrate size of 3" × 3" where high heat removal from ICs is required. A significant work pertinent to this domain is by Hajmohammdi and co-workers [1]. They numerically determined the optimal thickness of a conductive plate maintained between a cold-flowing fluid and a heated block. They found the temperature of the heated block depends on flow parameter (Re) and thermal conductivity. Hsu et al. [2] have presented mixed convection cooling of heated modules in a vertical wind tunnel

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numerically to show the dependence of the Nusselt number on the position of heaters and substrate thermal conductivity. Tseng et al. [3] Studied the cooling of heaters by natural convection and radiation effects by using the discrete ordinates method model. They found that the amount of thermal radiation is greater when the chipboard is in a vertical direction. Ledezma and Bejan [4] studied laminar natural convection cooling of staggered vertical plates and developed a correlation for optimal horizontal spacing. Meinders and Hanjalic [5] experimentally studied turbulent forced convection from two in-line, and staggered heated blocks mounted on a wall and found that the block-averaged heat transfer coefficient is independent of the relative placement of heaters. Jubran et al. [6] have experimentally studied the effects of rectangular block sizes in an array under forced convection cooling. They found a significant increase in Nusselt number using different sizes or shapes of blocks. Jadhav and Balaji [7] have performed combined experiments and simulations on fins in a vertical channel for electronic cooling. The authors found that pressure drop and thermal resistance depend on the pin-fin's diameter. Cheng et al.[8] studied the temperature field of the LED packaging substrate and found that role of spreading resistance was significantly affecting the temperature field. Bilen et al. [9] have conducted forced convection experiments for the cooling of heaters on a plate. They found that heater spacing and orientation are crucial in heat dissipation. Nardini and Paroncini [10] have conducted experiments to study heater size and location on cooling in a square wind tunnel. They found that effect of the heater's size and location change the flow velocity. Hadim and Bethancourt [11] numerically studied the forced convection cooling problem for a heater with a fluid-saturated porous medium. They found slight heat transfer enhancement, but significant pressure drops for increased heat source spacing. Refai and Yovanovich [12] studied the natural convection air cooling problem for a square enclosure with a heater and obtained a correlation between Nu and Ra. Yan et al. [13] identified a space-wise dependence of heat sources using the computational method and showed the method's effectiveness with numerical examples. Srikanth and Balaji [14] conducted experiments for pin heat sink with PCM for heaters of the identical area. They showed the significance of PCM on cooling. Chen and Liu [15] performed forced convection cooling experiments to study the effect of heat source spacing and found out optimal spacing ratio for 3 x 3 heaters. Durgam et al. [16-19] experimentally and numerically studied the cooling of heated modules in a wind tunnel by convection cooling. They found that the size and position of heaters, Reynolds number, and substrate conductivity are significant in the enhancement of heat transfer. Wang and Jaluria [20] have performed simulations to study heat dissipation from two flush heaters in a duct. The investigators found the conductance ratio, and the Reynolds numbers are significant in heat transfer. Deng [21] numerically investigated natural convection from the heater-sink pair in a vertical duct. They found that there is a close relation between total heat transfer and the number of eddies. Yilmaz and Gilchrist [22] performed combined experiments and simulations on the cooling of vertical plate channels. The authors observed that the numerical technique used to predict the temperature field is fairly good. Bejan and Sciubba [23] Investigated forced convection cooling of a bunch of parallel substrates in optimal spacing. They found that optimal spacing has a notable effect on surface temperature and rate of heat dissipation. Rafiee and Sadeghiazad [24] optimized the problem of heat mass transfer from hot and cold vortex tubes and found simulated and experimental values are a better match. Bejan et al. [25] have presented heat and fluid flow problems and optimal geometry of the flow channel. They found that an array of triangular elements reduces thermal resistance and increases dissipation. Hajmohammadi et al. [26] have studied varying heat flux scenarios under forced convection cooling and found enhancement in heat transfer by optimum heat flux distribution on the pipe wall. Hajmohammdai et al. [27] studied conjugate forced convection by inserting a thick plate of optimal thickness between the heated module and a cooling fluid and found a decrement in maximum temperature. Chinnov et al. [28] have conducted heat transfer experiments on a falling liquid film breakdown on a heater and found a good match of results with previous studies. Chinnov et al. [29] experimentally studied heat transfer from heat sources to the dielectric film, flowing over a plate inclined at different angles.They found the heat flux at which continuous film flow was disturbed, decreased with decreasing the plate inclination angle. Jaluria and Gupta [30] carried out experiments for a 4 x 3 heat source array with forced convection water cooling with specified heat input for each heat source array. They found higher rates of heat transfer for low channel heights. Jaluria and Papanicolaou [31] numerically studied mixed convection cooling from the heaters in a rectangular channel with a uniform surface heat flux input. They presented the temperature and flow fields in the channel. Bar-Cohen et al. [32] studied high heat flux liquid cooling of electronic modules using phase change liquids and found correlations to predict heat transfer coefficients. Incropera [33] provided comprehensive reviews on convective heat transfer options for thermal control of electronics. Kandlikar [34, 35] has presented an excellent review of technological developments in liquid and high heat flux chip cooling with single-phase flow in microchannels.

The literature shows that research is done on conjugate heat transfer with air cooling and liquid cooling for high heat densities. The studies on heat transfer enhancement through geometric modification of high heat flux IC chips on small substrates by forced convection air cooling are rare. Therefore, the main motives of this study are to find the effects of geometric modification, the effect of substrate thermal conductivity, size, positions, and spacing of IC chips on the thermal performance when generating high heat flux densities. The present study has significant heat

transfer applications in various fields where electronics cooling is indispensable.

NUMERICAL MODELING

Figure 1(a) shows a computational domain consisting of a substrate board of size 75 x 75 mm, mounted with nine discrete IC chips in a particular case. The chip location in each row on a substrate, the numbers specified are 11, 12, 13, 21, 22, 23, 31, 32, and 33. Both the lateral sides are assumed to be adiabatic. The air is flowing over IC chips in the direction along the x-axis, as shown by the arrowhead. Figure 2 shows the specifications of the IC chips viz. H11, H5, and H2 are the type of IC chips having a ratio of heat dissipated from 1, 2, and 3 rows in the proportion of 5:2:1. Table 1 shows specifications, including size and heat input to each IC chip. Twelve different chip sizes are used in the study. From the set of twelve, any nine IC chips of three other specifications are mounted on the substrates each time to study the heat dissipation from these IC chip combinations. The procedure used for numerical simulation using COMSOL Multiphysics 5.4 [36] following Durgam et al. [18] (to avoid repetition of the detailed description not given here). The model consists of nine silicon IC chips equipped on FR4, bakelite, single layer copper clad board (CCBSL), and multi-layer copper clad board (CCBML) of thermal conductivity of k = 0.3, 1.4, 8.8, and 40.5 W/m K, respectively. The lower thermal conductive substrates such as FR4 and bakelite are simulated for the heat flux of 5000 W/m^2 at a flowing air velocity of 2.5 m/s. The higher thermal conductive substrates such as CCBSL and CCBML use heat flux of 10000 W/m^2 with a flowing air velocity of 1.5 m/s for simulations.

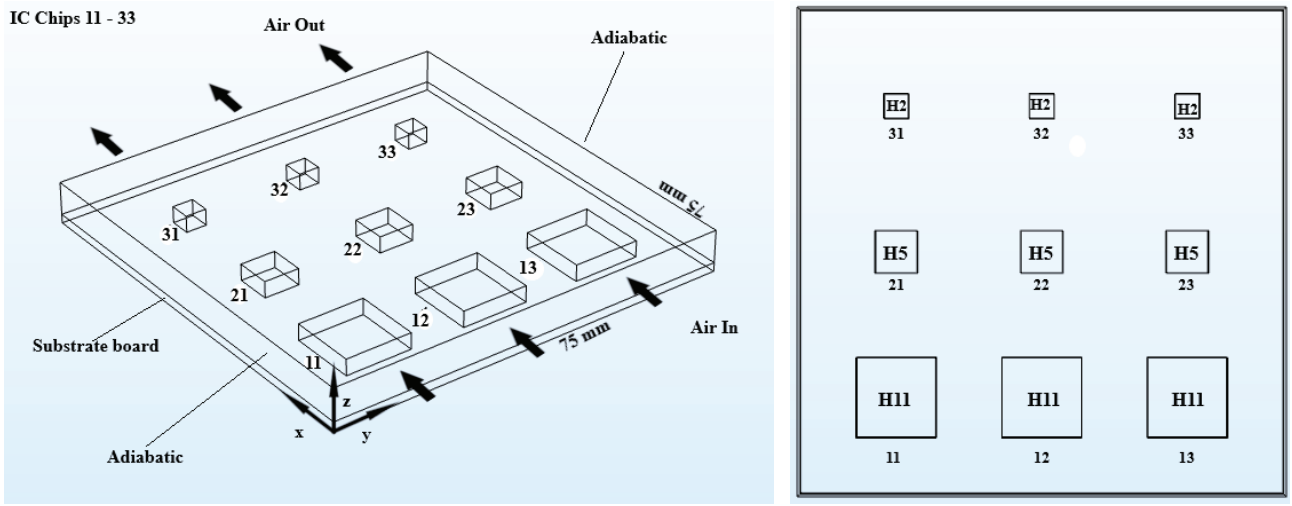
Table 1 shows the specifications of the chips, i.e., the number given to each chip, the size of the IC chip, and the heat added to each chip for q = 10000 W/m^2. IC chips with 12 different sizes are given numbers from H1 to H12 in increasing order. The slots on the substrate to place each chip are assigned numbers 11 to 33 [Figure 1(a)]. The smallest and largest size of the IC chips has given the heat of 0.55 and 3.3W, respectively.

Table 1. Description of the IC chips

Chip No.	Size of a chip (mm)	Heat, Q (W)
H1	3.5x3.5x3	0.55
H2	4x4x3	0.6
H3	5x5x3	0.86
H4	6x6x3	1.1
H5	6.5x6.5x3	1.2
H6	8x8x3	1.6
H7	9.5x9.5x3	2
H8	10x10x3	2.1
H9	10.5x10.5x3	2.4
H10	11.5x11.5x3	2.6
H11	12.5x12.5x3	3
H12	13x13x3	3.3

Table 2 shows seven configurations types considered in the study namely, A0 to F and the method of allocating the position to each IC chip on substrate board 11 to 33 and the type of IC chip to be used for the controlled amount of heat dissipated through each row (Table 1).

Table 3 shows the amount of heat dissipated from each row for all seven configurations to have total heat removed from each row, the overall heat dissipation and heat flux in each row is kept constant by maintaining the size and



(a) **(b)**

Figure 1. (a) Numerical model and (b) Configuration.

Table 2. Position of IC chips in each configuration

Cases	Chip position (11,12,13)	Chip position (21, 22, 23)	Chip position (31, 32, 33)
A0	H6	H6	H6
A	H7	H6	H5
B	H8	H6	H4
C	H9	H6	H3
D	H10	H6	H1
E	H11	H5	H2
F	H12	H3	H2

Table 3. Heat dissipated from each configuration

Cases	Ratio of the heat removed	Heat removed from row 1 (W)	Heat removed from row 2 (W)	Heat removed from row 3 (W)
A0	1:1:1	4.8	4.8	4.8
A	5:4:3	6	4.8	3.6
B	4:3:2	6.4	4.8	3.2
C	3:2:1	7.2	4.8	2.4
D	5:3:1	8	4.8	1.6
E	5:2:1	9	3.6	1.8
F	5.5:1.4:1	10	2.6	1.8

location of chips. The different configurations with different heat dissipation ratios are labeled as case A0 to F.

Governing Equations

The software uses governing equations such as continuity (Eq. 1), momentum (Eqs. 2 - 4), and energy equation (Eq. 5) for numerical simulations.

Fluid region: Equation of continuity

$$\frac{\partial(u)}{\partial x}+\frac{\partial(v)}{\partial y}+\frac{\partial(w)}{\partial z}=0 \quad (1)$$

X-momentum equation

$$u\frac{\partial u}{\partial x}+v\frac{\partial u}{\partial y}+w\frac{\partial u}{\partial z}=-\frac{1}{\rho}\frac{\partial p}{\partial x}+\frac{\mu}{\rho}\left[\frac{\partial^2 u}{\partial x^2}+\frac{\partial^2 u}{\partial y^2}+\frac{\partial^2 u}{\partial z^2}\right] \quad (2)$$

Y-momentum equation

$$u\frac{\partial v}{\partial x}+v\frac{\partial v}{\partial y}+w\frac{\partial v}{\partial z}=-\frac{1}{\rho}\frac{\partial p}{\partial y}+\frac{\mu}{\rho}\left[\frac{\partial^2 v}{\partial x^2}+\frac{\partial^2 v}{\partial y^2}+\frac{\partial^2 v}{\partial z^2}\right] \quad (3)$$

Z-momentum equation

$$u\frac{\partial w}{\partial x}+v\frac{\partial w}{\partial y}+w\frac{\partial w}{\partial z}=-\frac{1}{\rho}\frac{\partial p}{\partial z}+\frac{\mu}{\rho}\left[\frac{\partial^2 w}{\partial x^2}+\frac{\partial^2 w}{\partial y^2}+\frac{\partial^2 w}{\partial z^2}\right] \quad (4)$$

Solid region: The energy equation

$$u\frac{\partial T}{\partial x}+v\frac{\partial T}{\partial y}+w\frac{\partial T}{\partial z}=\alpha\left[\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}\right] \quad (5)$$

Nusselt number, Nu is calculated using Eq. 6 and given by

$$Nu=\frac{hL}{k} \quad (6)$$

The size of the substrate is 75x75 mm. The thickness of low thermal conductivity substrates i.e FR4 and the bakelite is 4 mm. Whereas the higher thermal conductivity substrates i.e., single and multi-layer CCB, is 1.6 mm. The air layer 6 mm above the board is used [36]. The following assumptions are made in this study:

(1) Steady-state conditions;
(2) Isothermal IC chips;
(3) Top, bottom boundaries, side surfaces, and edges are adiabatic;
(4) Negligible heat transfer by radiation.
(5) Negligible viscous dissipation.

The material properties at 27 °C and 1 atm. are described in Table 4.

Grid Independent Study

Grid independent studies have been performed for software-generated free tetrahedral mesh with grids ranging

Table 4. Thermophysical properties of materials

Material	k (W/m K)	ρ (kg/m^3)	Cp (J/kg K)
FR4	0.30	1890	900
Bakelite	1.40	1290	1460
CCBSL	8.80	2048	1370
CCBML	40.50	2580	1280
Silicon	148	2329	700

Forced convection BC's: x = 0, T = T_∞, and u = u_o = 1.5, or 2.5 m/s. x = L, p = p_o (zero pressure BC). Lateral boundaries are adiabatic.

Table 5. Grid sensitivity study

Element growth rate	No. of grids	T (°C)	% Δ T
1.4	222,425	80.45	-
1.35	247,510	80.67	0.27
1.3	272,572	80.88	0.26
1.25	298,308	81.11	0.28
1.2	322,580	81.25	0.17

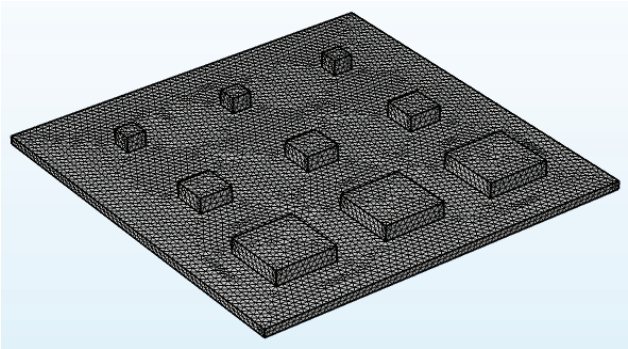


Figure 2. Mesh for IC chips and substrate board.

from 222,425 to 322,580, i.e., from fine to extra coarse. The coarse mesh has 272,572 grids. The meshing time required is 6.28 s, and the quality for minimum elements is 0.0778. The results of temperature and percentage change in temperature for different numbers of grids are shown in Table 5. Figure 2 shows the type of mesh used for the study. The blend factor value of 1.0 for the second-order discretization solver is considered that yield better convergence and higher accuracy of results.

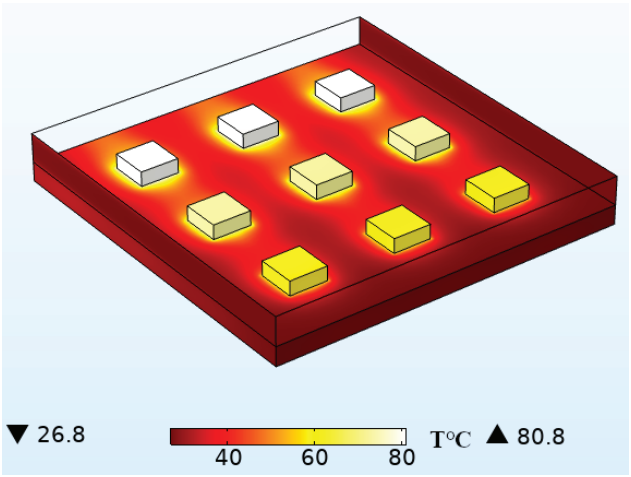
RESULTS AND DISCUSSION

The main objective of this contemporary idea of modifying the geometric distance and size of IC chips is to dissipate heat from electronic devices for optimal thermal performance. The study is carried out for heat transfer enhancement using a different type of configurations having different sizes of chips maintained in each row. Heat transfer characteristics are closely related to the thermal conductivity of the substrate board. Better thermal performance is observed by using a higher thermal conductive substrate. Steady-state numerical simulations by selecting conjugate heat transfer module are performed using COMSOL Muliphysics 5.4. FR4, bakelite, CCBSL, and CCBML are used as substrate materials for the study. For FR4 and bakelite, numerical simulations were performed for the heat flux of 5000 W/m^2 at air velocity of 2.5 m/s. For CCBSL, CCBML were simulated for heat flux 10000 W/m^2 at an air velocity of 1.5 m/s. The lower thermal conductance substrates like FR4 and bakelite cannot withstand the higher heat flux values at lower air velocities, as obtained from the previous studies [16].

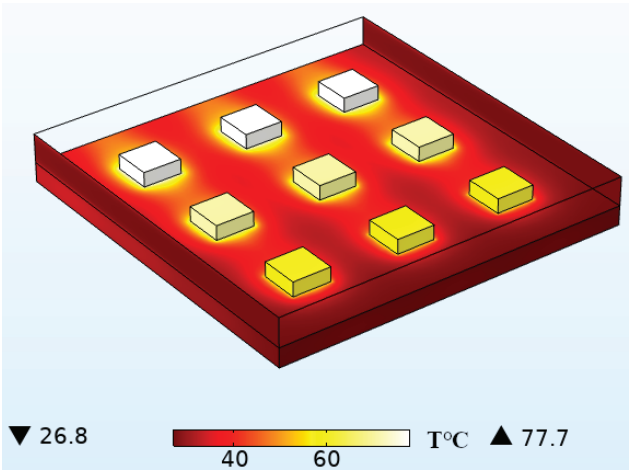
Heat Transfer Enhancement by Chip Size Modifications

Initially, numerical study has carried out for all the square IC chips for all substrates used in this investigation. Figure 3 shows the temperature plot for low thermal conductivity substrate material FR4 using all square IC chips at uniform heat flux, q = 5000 W/m^{2,} and air velocity, u_o = 2.5 m/s. For FR4 and bakelite, maximum temperatures are observed to be 80.8 and 77.7 °C, respectively. The maximum temperature is monitored for IC chip placed at the middle in the third row i.e., location 32 on the substrate and configuration case A0. The temperatures plot indicates that the maximum temperatures are decreased using higher thermal conductivity substrate board material.

The simulations are performed for the same heat inputs and velocities using different configurations to study and compare the heat transfer performance. Figure 4 shows temperature and temperature contour plots for FR4 and



(a)



(b)

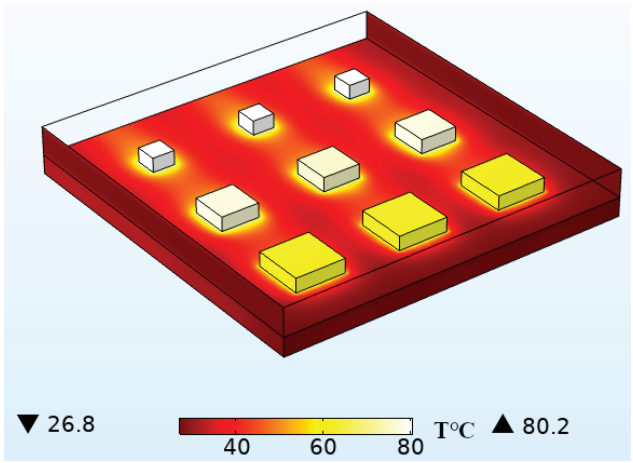
Figure 3. Temperature plots for (a) FR4 and (b) bakelite using (case A0), 5000 W/m^2, 2.5 m/s.

bakelite for configuration case C at q = 5000 W/m^2 and u_o = 2.5 m/s. The total heat removed from each row 1, 2, and 3 using all configuration cases A0 – F are shown in Table 3. The heat dissipated (Q) from any configuration is 14.4 W, but in different ratios from each row for cases A - F. In configuration case C, heat is consumed in the proportion 3:2:1, i.e., 3.6 W heat is removed from row 1, 2.4 W from row 2, and 1.2 W from row 3. It is noteworthy that half of the total heat was removed from the first row.

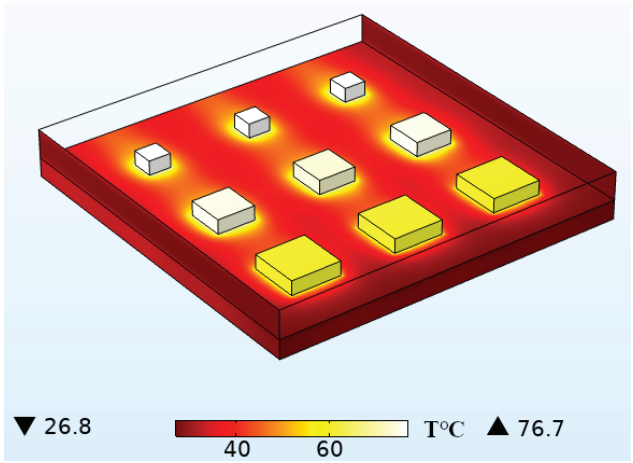
The maximum temperatures on the substrate is decreased by 0.6 °C and 1°C for FR4 and bakelite compared with all nine square IC chips in configuration case A0. It indicates heat transfer enhancement in FR4 and bakelite is due to chip size modifications, location, and substrate thermal conductivity.

Effect of Chip Size and Substrate Thermal Conductivity on Maximum Temperature

Figure 5 shows temperature plot for CCBSL and CCBML using all nine square IC chips, configuration case A0 with a q = 10000 W/m^2, at u_o = 1.5 m/s. The maximum temperature observed in the case of CCBSL and CCBML is 86.9 °C and 76 °C, respectively. The chip in the middle of



(a)



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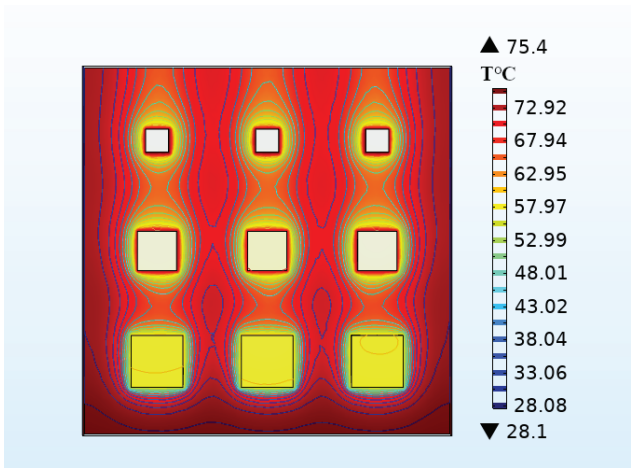
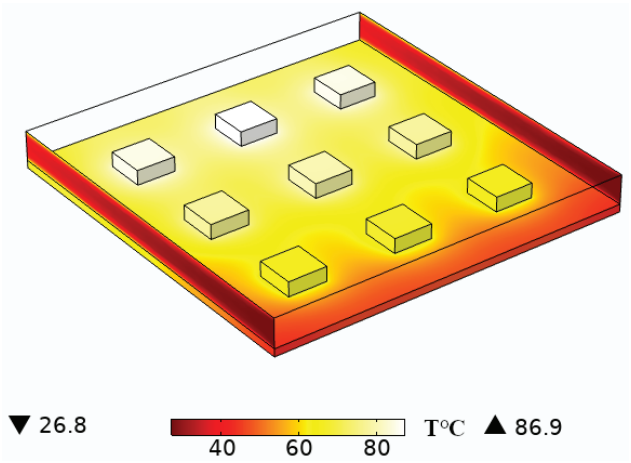
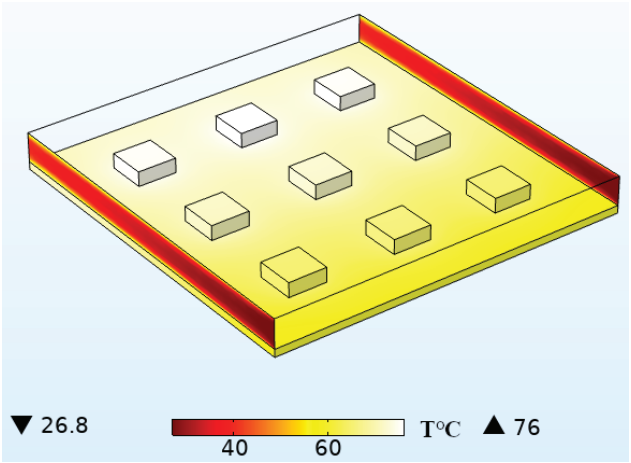


(c)

Figure 4. Temperature ptot (a) FR4, (b) bakelite and (c) temperature contour plot for bakelite using (case C), 5000 W/m^2, 2.5 m/s.



(a)

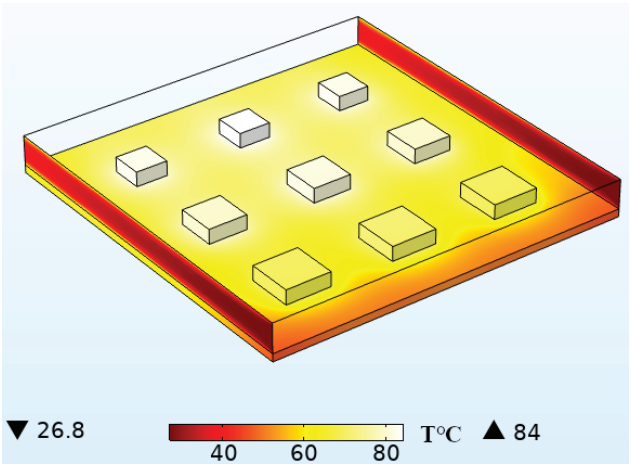


(b)

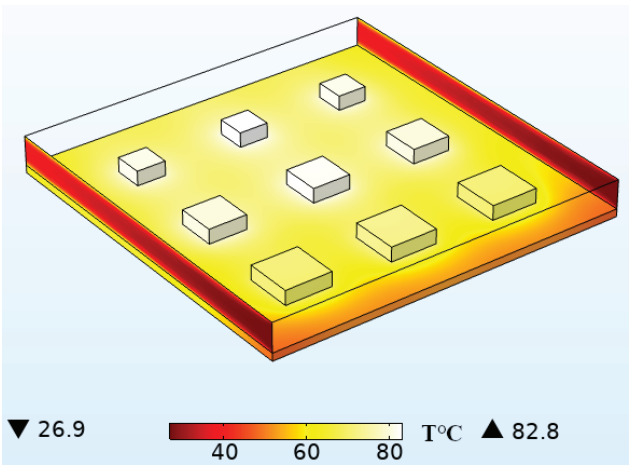
Figure 5. Temperature plots (a) CCBSL and (b) CCBML for case A0, 10000 W/m^2, 1.5 m/s.

the third row has the maximum temperature. Furthermore, it was observed that the maximum temperature decreased using higher thermal conductivity substrate material, i.e., CCBML. It is also noticed that IC chips in each row of configuration case A0 are dissipating the same amount of heat, i.e., 4.8 W, but the IC chips placed in the third-row results in maximum temperature compared with the other two rows [18]. For the same heat input and the velocity, there is a reduction of 10.9 °C using CCBML i.e decrease of maximum temperature on board by using a substrate of higher thermal conductivity.

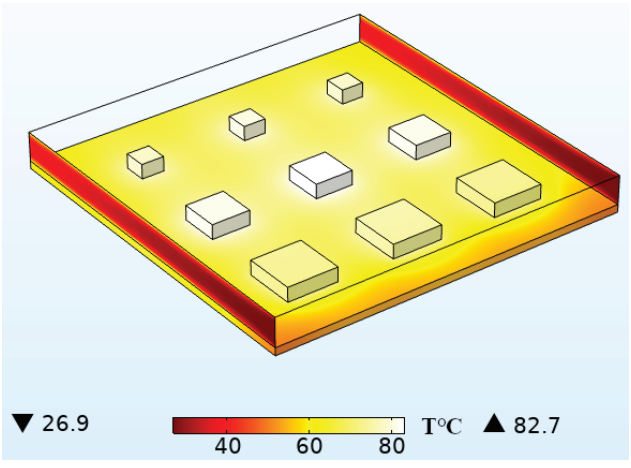
The temperature plots for configuration cases A, B, and C using CCBSL for u_o = 1.5 m/s and q = 10000 W/m^2 are as noticed in Figure 6. The results of case A0 are compared for the same heat input, air velocity, and substrate material with other cases from A to F to obtain desired enhanced heat transfer considering case C. Half of the total heat is removed from the first row in this configuration. The maximum temperature is reduced using case C instead of A0.



(a) Case A



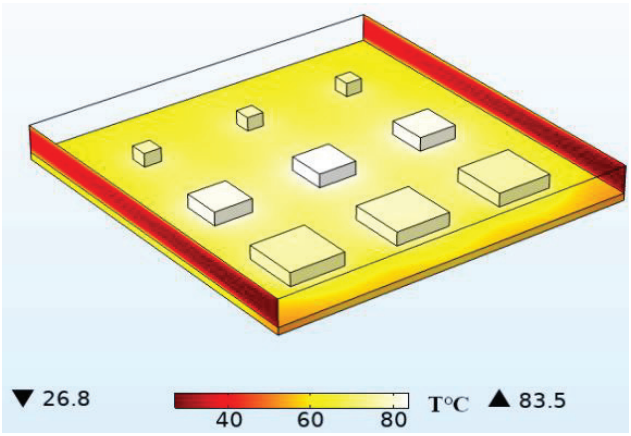
(b) Case B



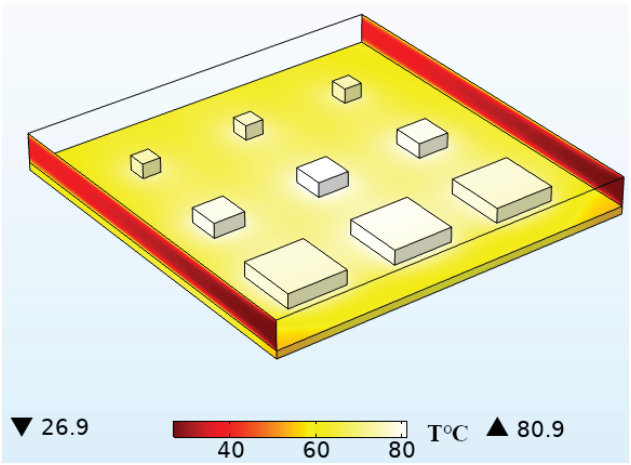
(c) Case C

Figure 6. Temperature plots for cases A, B and C using CCBSL for 10000 W/m^2, 1.5 m/s.

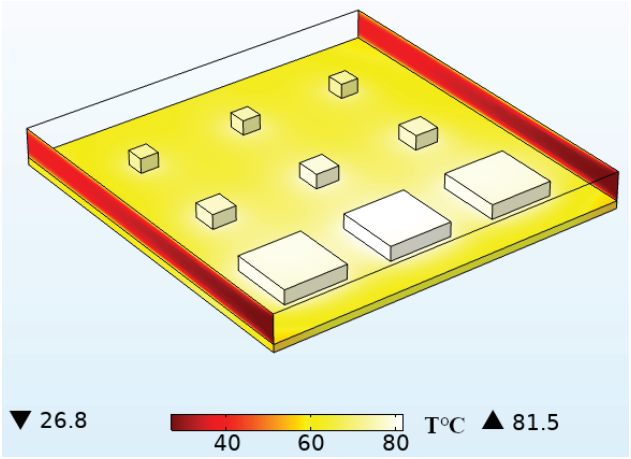
In case of CCBSL temperature is dropped from 86.9 °C [Figure 5(a)] to 82.7 °C [Figure 6(c)], while in case of CCBML it is dropped from 76 [Figure 5(b)] to 73.5 °C [Figure 9(a)].The maximum temperatures on the substrate



(a) Case D



(b) Case E



(c) Case F

Figure 7. Temperature plots of cases D, E and F using CCBSL for 10000 W/m^2, 1.5 m/s.

board are decreased by 4.2°C and 3.5°C for CCBSL and CCBML, respectively. Figure 7 shows the Temperature plots of cases D, E, and F using CCBSL for 10000 W/m^2, 1.5 m/s. It was found that case E results in the lowest temperature among all cases.

Figure 8 show the variation of Nusselt number with row number for cases A0, C, and E, at q = 10000 W/m^2 and u_o = 1.5 m/s. It is noticed that Nusselt number is higher for cases C and E for the first row, while in the second and third rows, it is less than cases A0. It is evidence of heat transfer enhancement by increasing heat dissipated from the first row. Numerical results are used to check the trend of these ratios for CCBML.

The velocity and temperature plot using CCBML for case E are shown in Figure 9. The air velocity at inlet is 1.5 m/s, whereas the maximum velocity at outlet is 2.43 m/s. The red lines shown in the velocity plot are the streamlines [Figure 9 (a)]. It follows the same trend compared with CCBML. The maximum temperature obtained for case F is 73.1°C that is the minimum compared with all cases from A0 to F.

The numerical results for all cases A0 - F using CCBSL and CCBML are studied. In cases A and B, the heat dissipated from the first row is less than half; for case C, it is precisely half, and for cases D, E, F, it is more than half. From the comparison of results with all the square IC chips case A0, the maximum temperature on the substrate decreases as heat dissipated from initial rows increases. But this decrease is up to a specific limit. At configuration case E, the temperature occurred is minimum, and hence the, case E is optimal. This geometry and chip sizes for the same heat flux, velocity, and heat dissipated results in heat transfer enhancement. Again, for case F, the highest temperature on the substrate increases. Heat transfer coefficients are based on these temperatures to obtain Nusselt numbers and plotted for all cases and shown in Figure 10. The configuration E results in the maximum value of Nu (Eq. 6).

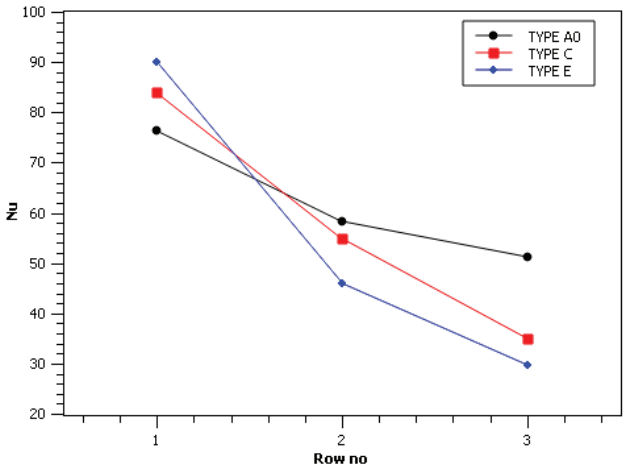
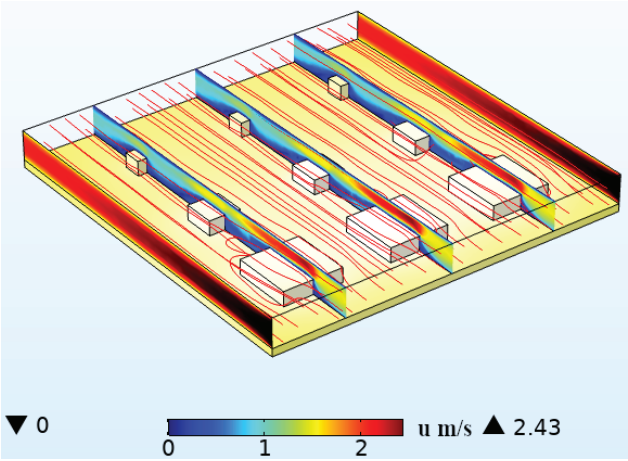
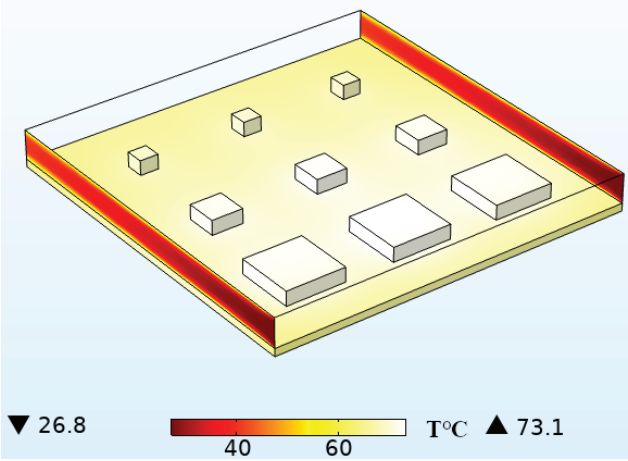


Figure 8. Variation of Nu with row number plot for cases A0, C, E for q = 10000 W/m^2 and u_o = 1.5 m/s.



(a) Velocity plot, Case E, CCBML



(b) Case E, CCBML

Figure 9. Velocity and temperature plots of case E using CCBML for q = 10000 W/m^2, u_o = 1.5 m/s.

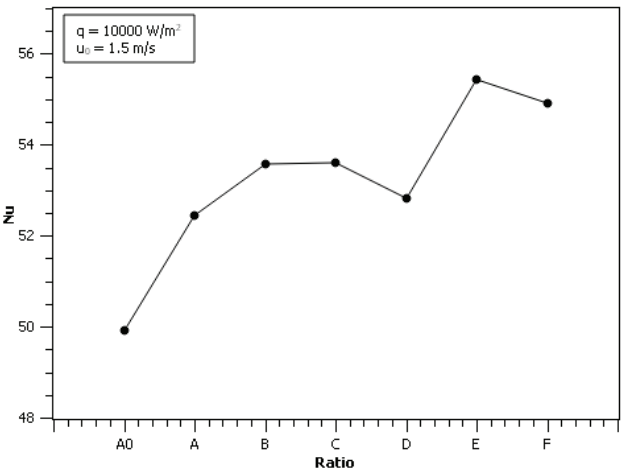


Figure 10. Variation of Nusselt number with heat ratio for cases A0 - F using q = 10000 W/m^2 and u_o = 1.5 m/s.

Effect of Substrate Conductance on Heat Transfer Enhancement

The effect of substrate conductance for configuration E was studied. Figure 11 shows the change in Nusselt number with rows using CCBSL and CCBML for q = 10000 W/m^2 and u_o = 1.5 m/s. It shows that Nu decreases from the first to the third row for both the substrate materials. The Nu is higher in the case of CCBML than that of CCBSL in all three rows.

The higher Nusselt number indicates of heat transfer enhancement due to increased substrate thermal conductivity.

Figure 12 shows the variation of temperature in chips for case E. It shows that temperature distribution is more uniform for CCBML than CCBSL. The uniform temperature distribution results in lower thermal stresses, prolonging the equipment's life. The temperatures obtained in CCBSL are lower compared with that of CCBML.

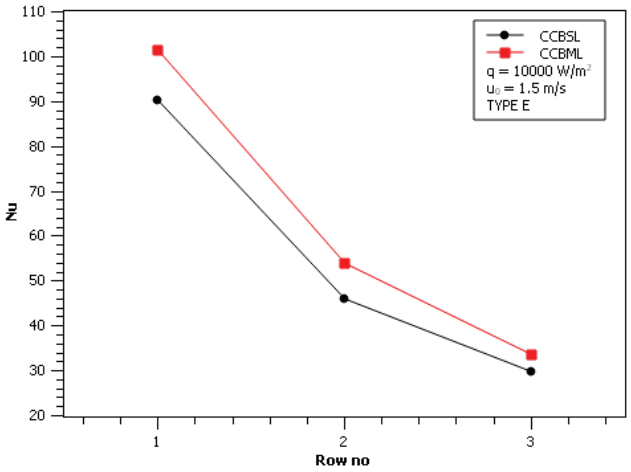


Figure 11. Nu we v/s row no for case E, for q = 10000 W/m^2 and u_o = 1.5 m/s.

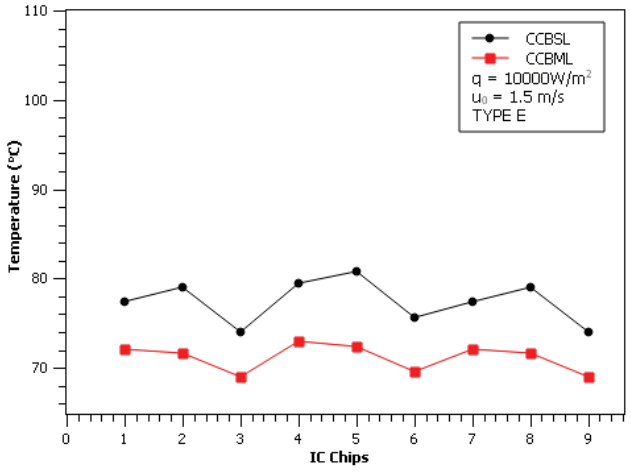
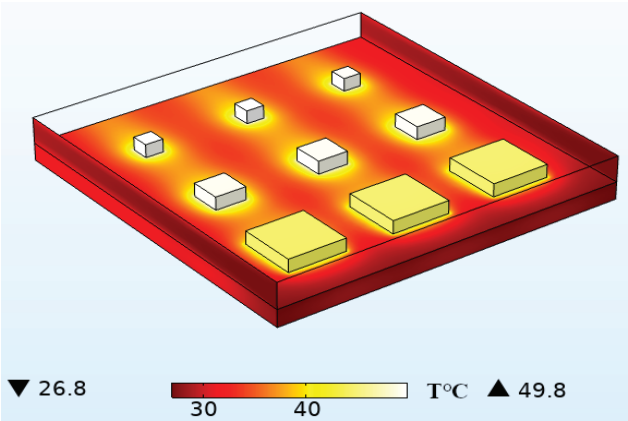


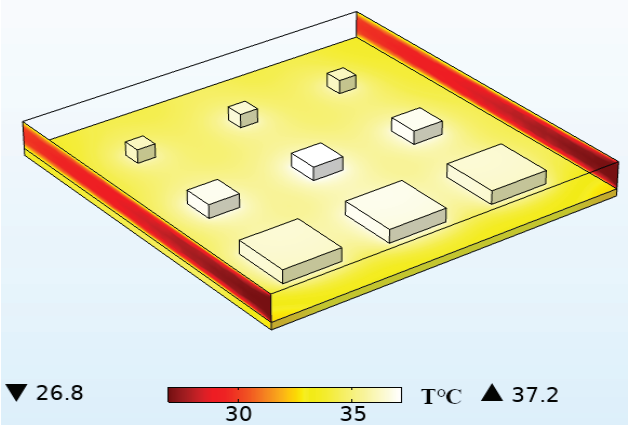
Figure 12. Variation of temperatures in IC chips for case E using CCBSL and CCBML for q = 10000 W/m^2 and u_o = 1.5 m/s.

Validation of Numerical Study with Previous Experimental Results

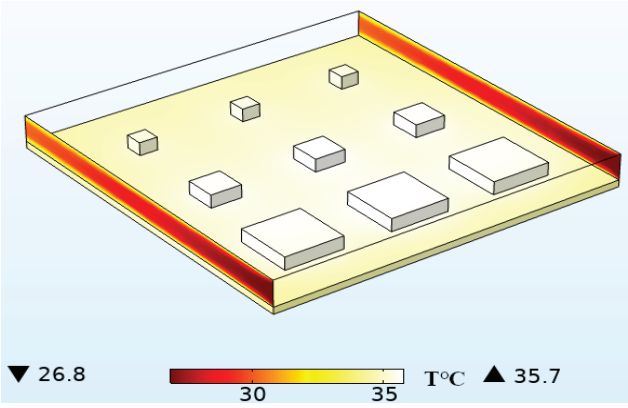
Figure 13 shows temperature plots for substrate materials as bakelite, CCBSL, CCBML for u_o = 1m/s and q = 1500 W/m^2. It is noticed from the results that the maximum temperatures are 49.8, 37.2, 35.7 °C in the case of bakelite, CCBSL, and CCBML. The high thermal conductance results in a reduction in the maximum temperature.



(a) bakelite



(c) CCBSL



(d) CCBML

Figure 13. Temperature plots (a) bakelite, (b) CCBSL and (c) CCBML at q = 1500 W/m^2, and u_o = 1m/s.

However, there in uniform temperature distribution in case of higher thermal conductivity substrate i.e CCBSL and CCBML. For bakelite, the maximum temperature exists for the IC chip with position 32. In the case of CCBSL and CCBML it occurred in the middle in the second row. But the temperature variation in all three IC chips in the second row is marginal. Chen and Liu [15] conducted experiments for the configuration with a 3x3 array to study the effect of spacing for Reynolds number values between 465 – 1560. The present work is compared for a uniform heat flux of 1500 W/m^2. Numerical results validated with the experimental data for the case S2/S1 = 1 (TYPE 1) for same values of q = 1500 W/m^2 and uo = 1 m/s. For carrying these simulations, the thickness of the backelite substarte board is considered 4 mm, while for CCBSL, CCBML it is to be considered of 1.6 mm. The oppresent placement of IC chips are analyased for different thermal conductive substrates to check its effect on maximum temperature and distribution. The similar temperature trend are followed for all the materials. The maximum temperature is minimum in the case E of the present study. The temperature values in the present study are quite good for the same heat flux value, substrate board material, and Reynolds number. Figure 14 indicates that the maximum tempearture are lower in case of higher thermal conductive like CCBSL and CCBML. Also, there is uniform temperature distribution.

Size of the substrate in the previous work [Ref. 15] is five times than in the present work. It is an indication of better thermal performance with less substrate area. There is substantial miniaturization in the present work as in [Ref. 15]. The temperatures obtained in the present work are lower, which leads to better performance and an increase in the life of electronic equipment.

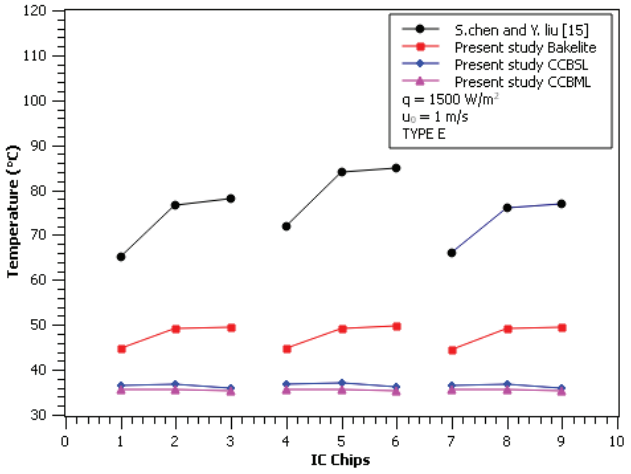
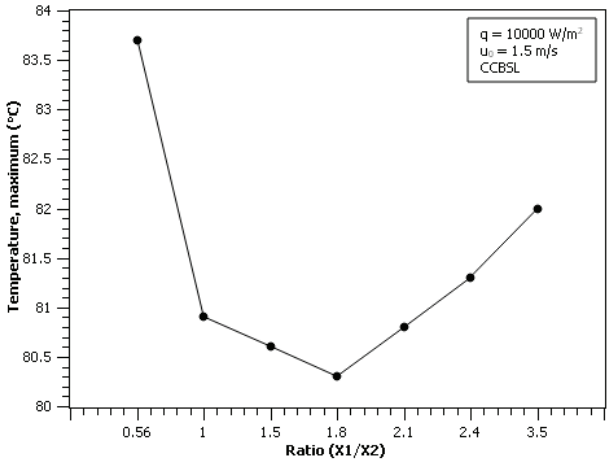


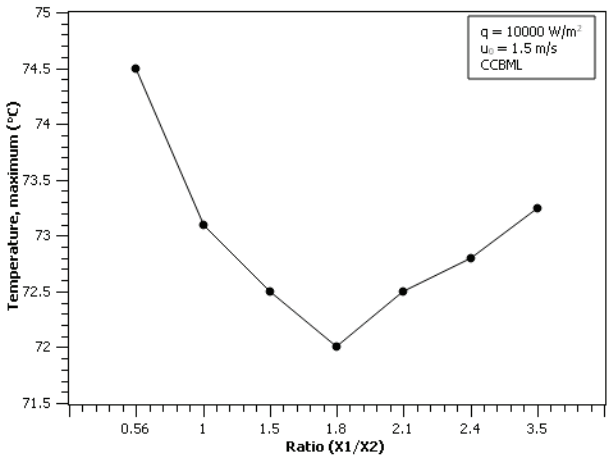
Figure 14. Temperature variations with IC chips plot for bakelite, CCBSL and CCBML for u_o = 1 m/s and q = 1500 W/m^2.

Effect of Optimum Spacing Ratio on Temperature

The variation of maximum temperature for each geometric ratio for CCBSL and CCBML using q = 10000 W/m^2 and u_o = 1.5 m/s are shown in Figure 15 (a) and (b). Chen Liu [15] used different geometric ratios of S2/S1 = 1, 1.3, 1.5, 1.8 to check the effect of IC Chip's spacing on heat dissipation and predicted enhancement of heat transfer when the spacing between rows follows geometric ratio. Following similar procedure, different geometric ratios of 0.56, 1, 1.5, 1.8, 2.1, 2.4, and 3.5 are used. The maximum heat dissipation occurred in case E. Therefore case E is optimal for maximum heat dissipation from three rows for q = 10000 W/m^2 and u_o = 1.5 m/s. It is observed that for spacing ratio, X1/X2 = 1.8 the maximum temperatures are least for CCBML and CCBSL among the spacing ratios studied.



(a) CCBSL



(b) CCBML

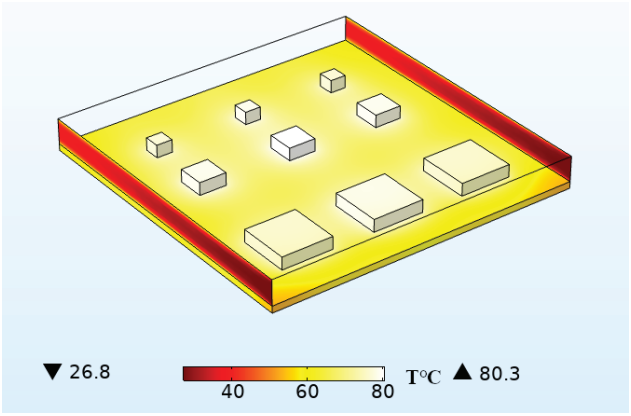
Figure 15. Maximum temperatures v/s geometric ratios for (a) CCBSL and (b) CCBML for u_o = 1.5 m/s, and q = 10000 W/m^2.

Shifting Second Row Towards First

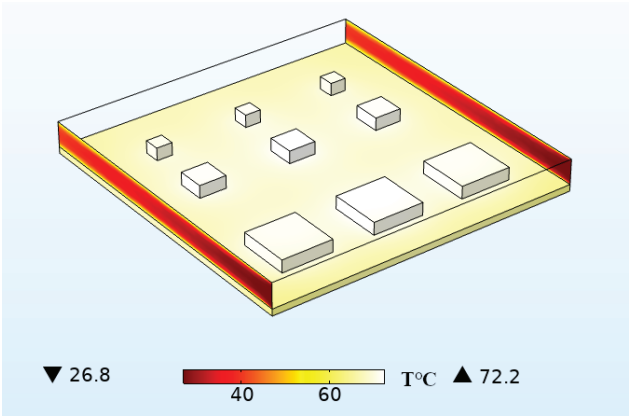
Two types of modifications are possible, i.e., by shifting the second row towards the first row and moving the second row towards the third row. These shifting of rows in both directions are considered to confirm the effect of the geometric position of IC chips on heat dissipation. In the case of geometric ratio X1/X2 = 0.56 the maximum temperature on the substrate board increased. Shifting the second row towards the first will result in increased temperature; hence this shifting of the second row towards the first is not preferable.

Shifting the Second Row Towards the Third Row

The geometric ratios X1/X2 = 1.5, 1.8, 2.1, 2.4, 3.5 are considered to check the effect of spacing in optimal configuration i.e., case E, which is obtained from optimal heat distribution. It is observed that there is a decrease in temperature compared with X1/X2 = 0.56. It indicates that shifting of second-row towards third is beneficial for the heat transfer point of view compared with shifting towards the first row. Large-sized IC chips placed in the first row give a lower temperature. The study for spacing ratio 1.8 showed that the temperature drop occurs when moved



(a)



(b)

Figure 16. Temperature °C, (X1/X2) = 1.8, (a) CCBSL and (b) CCBML (case E), q = 10000 W/m^2, u_o = 1.5 m/s.

to 1.8 from 1.5. For different geometric proportions 2.1, 2.4, 3.5, the highest temperature on the substrate board is increased [Figure 15]. It indicates that X1/X2 = 1.8 is the optimal spacing ratio. Compared with the FR4 and bakelite, the single and multi-layer copper clad boards result in lower temperatures due to their higher thermal conductivity. The heat dissipation from the substrate also strongly depends on heat source size and location. Chen and Liu [15] also proposed that the optimal geometric ratio is 1.8; the results are very well-validated with previous experimental work. In case of Chen and Liu [15] authors have worked on the shifting of rows when all the heaters are dissipating same amount of heat and flux. Authors observed that shifting of second row towards first were beneficial in their study. In the present study heaters in subsequent rows are dissipating different amount of heat. As maximum heat is tried to be extracted in the initial rows. Due to maximum heat dissipation in initial rows, saturation point for the air layer near the heaters is reached and now air will not cool heaters effectively. When shifitng towards the third row air will get a sufficient time to transfer the heat towards adjacent layers. That optimum heat transfer will take place till the spacing ratio 1.8. Figure 18 shows the temperature plots for optimal geometric ratio with CCBSL, CCBML as substrate material. It also clarifies that the maximum temperature dropped using a higher thermal conductivity substrate.

CONCLUSION

From the study of geometric modification and placement of high flux IC chips on substrates of different materials for enhanced heat transfer following are the conclusions:

1. Bakelite substrate gives lower temperatures than FR4 for the equal heat flux of 5000 W/m^2 and 2.5 m/s air velocity. Similarly, temperatures obtained using CCBML for heat flux of 10000 W/ m^2 and air velocity of 1.5 m/s in all cases are lower than all substrates used in the study. CCBSL and CCBML, give uniform temperatures on the substrate board, reducing thermal stresses.
2. Results showed that the substrate board's temperature depends upon the size and placement of IC chips, heat flux density, substrate thermal conductivity, and Reynolds number. Placing larger IC chips at the bottom row and decreasing sizes in the second and third rows give lower temperatures. Furthermore, the spacing between rows plays a vital role in temperature on substrates. Case E gives minimum temperature compared with all cases A0 – F considered in the study with an optimal spacing of 1.8 using CCBSL results in heat transfer enhancement
3. It is proposed that placing larger-sized electronic chips in the initial row results in an increased Nusselt number in the first row. In contrast, there is a reduction in the Nusselt number in the subsequent rows. It gives a significantly enhanced heat transfer. This work is helpful in the electronic industry, where IC Chips generate high heat fluxes for high thermal conductivity substrates.
4. This configuration is suitable for electronic equipment dissipating 15 W. Multiple substrates may be used for high values of heat rejection

NOMENCLATURE

IC	Integrated Circuit
L	Length of heat source
Nu	Nusselt number
Re	Reynolds number
ΔT	Excess temperature of the air, ($T - T_\infty$), °C
X1	Central distance between first and second rows.
X2	Central distance between second and third rows

AUTHORSHIP CONTRIBUTIONS

Authors equally contributed to this work.

DATA AVAILABILITY STATEMENT

The authors confirm that the data that supports the findings of this study are available within the article. Raw data that support the finding of this study are available from the corresponding author, upon reasonable request.

CONFLICT OF INTEREST

The author declared no potential conflicts of interest with respect to the research, authorship, and/or publication of this article.

ETHICS

There are no ethical issues with the publication of this manuscript.

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